Commercial and Industrial DDR4 8Gb SDRAM

Features

- **Data Integrity**
  - Auto Self Refresh (ASR) by DRAM built-in TS
  - Auto Refresh and Self Refresh Modes
- **DRAM Access Bandwidth**
  - Separated IO gating structures by Bank Groups
  - Self Refresh Abort
  - Fine Granularity Refresh
- **Signal Synchronization**
  - Write Leveling via MR settings[1]
  - Read Leveling via MPR
- **Reliability & Error Handling**
  - Command/Address Parity
  - Databus Write CRC
  - MPR readout
  - Boundary Scan (X16)
  - Post Package Repair
- **Signal Integrity**
  - Internal VREFDQ Training
  - Read Preamble Training
  - Gear Down Mode
  - Per DRAM Addressability
  - Configurable DS for system compatibility
  - Configurable On-Die Termination
  - Data bus inversion (DBI)
  - ZQ Calibration for DS/ODT impedance accuracy via external ZQ pad (240 Ω ± 1%)
- **Power Saving & Efficiency**
  - POD with VDDQ termination
  - Command/Address Latency (CAL)
  - Maximum Power Saving
  - Low-power Auto Self Refresh (LPASR)

Programmable Functions

- **Output Driver Impedance (34/48)**
- **CAS Write Latency (9/10/11/12/14/16/18/20)**
- **Additive Latency (0/CL-1/CL-2)**
- **$\overline{CS}$ to Command Address Latency (3/4/5/6/8)**
- **Command Address Parity Latency (4/5/6)**
- **Write Recovery Time (10/12/14/16/18/20/24)**
- **Burst Type (Sequential/Interleaved)**
- **RTT_PARK (34/40/48/60/80/120/240)**
- **RTT_NOM (34/40/48/60/80/120/240)**
- **RTT_WR (80/120/240)**
- **Read Preamble (1T/2T)**
- **Write Preamble (1T/2T)**
- **Burst Length (BL8/BC4/BC4 or 8 on the fly)**
- **LPASR (Manual: Normal/Reduced/Extended, Auto:TS)**

Options

- **Temperature Range (T_c) [5]**
  - Commercial Grade : 0℃~95℃
  - Industrial Grade (-I) : -40℃~95℃
  - Quasi Industrial Grade (-T) : -40℃~95℃
- **VDD/VDDQ/VPP**
  - 1.2V / 1.2V / 2.5V

- **Package information**

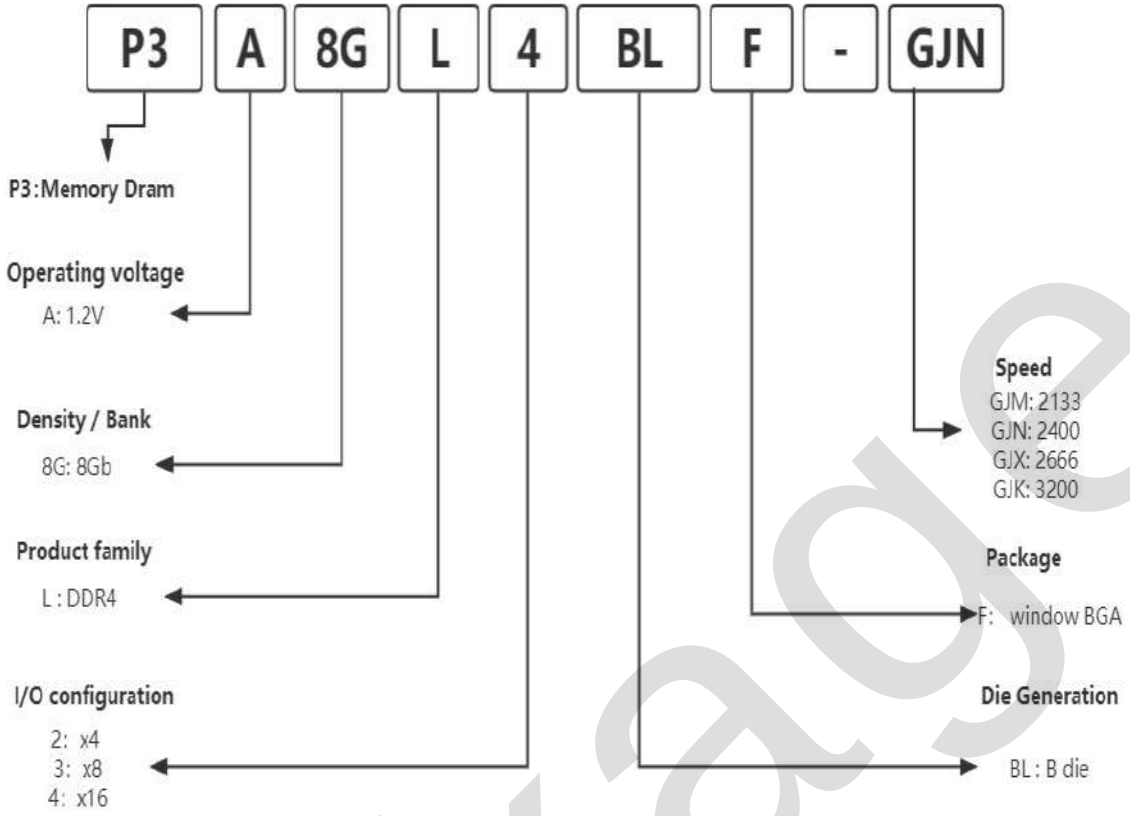
Lead-free RoHS compliance and Halogen-free

TFBGA Package	Dimension (mm)	Ball pitch (mm)
78-Ball	7.50 x 12.00	0.80
96-Ball	7.50 x 13.00	0.80

- **Density and Addressing**

Organization	1024Mb x 8	512Mb x 16
Banks	4 (BA[1:0])	4 (BA[1:0])
Bank Groups	4 (BG[1:0])	2 (BG[0])
Row Address	A[15:0]	A[15:0]
Column	1K (A[9:0])	1K (A[9:0])
Page Size	1KB	2KB
tREFI [3]	Tc≦85℃:7.8μs, Tc>85℃:3.9μs	
tRFC [4]	260ns	

NOTE 1 Write Leveling feedback should be given on all data bits in parallel.
NOTE 2 For the same organization and voltage, the timing specification of high speed bin is backward compatible with low speed bin.
NOTE 3 Violating tREFI is not guaranteed.
NOTE 4 Violating tRFC is not guaranteed.
NOTE 5 When operate above 95℃ ,AC/DC will be derated.


P3 A 8G L 4 BL F - GJN
P3:Memory Dram
Operating voltage
A: 1.2V
Density / Bank
8G: 8Gb
Product family
L : DDR4
I/O configuration
2: x4
3: x8
4: x16
Speed
GJM: 2133
GJN: 2400
GJX: 2666
GJK: 3200
Package
F: window BGA
Die Generation
BL : B die

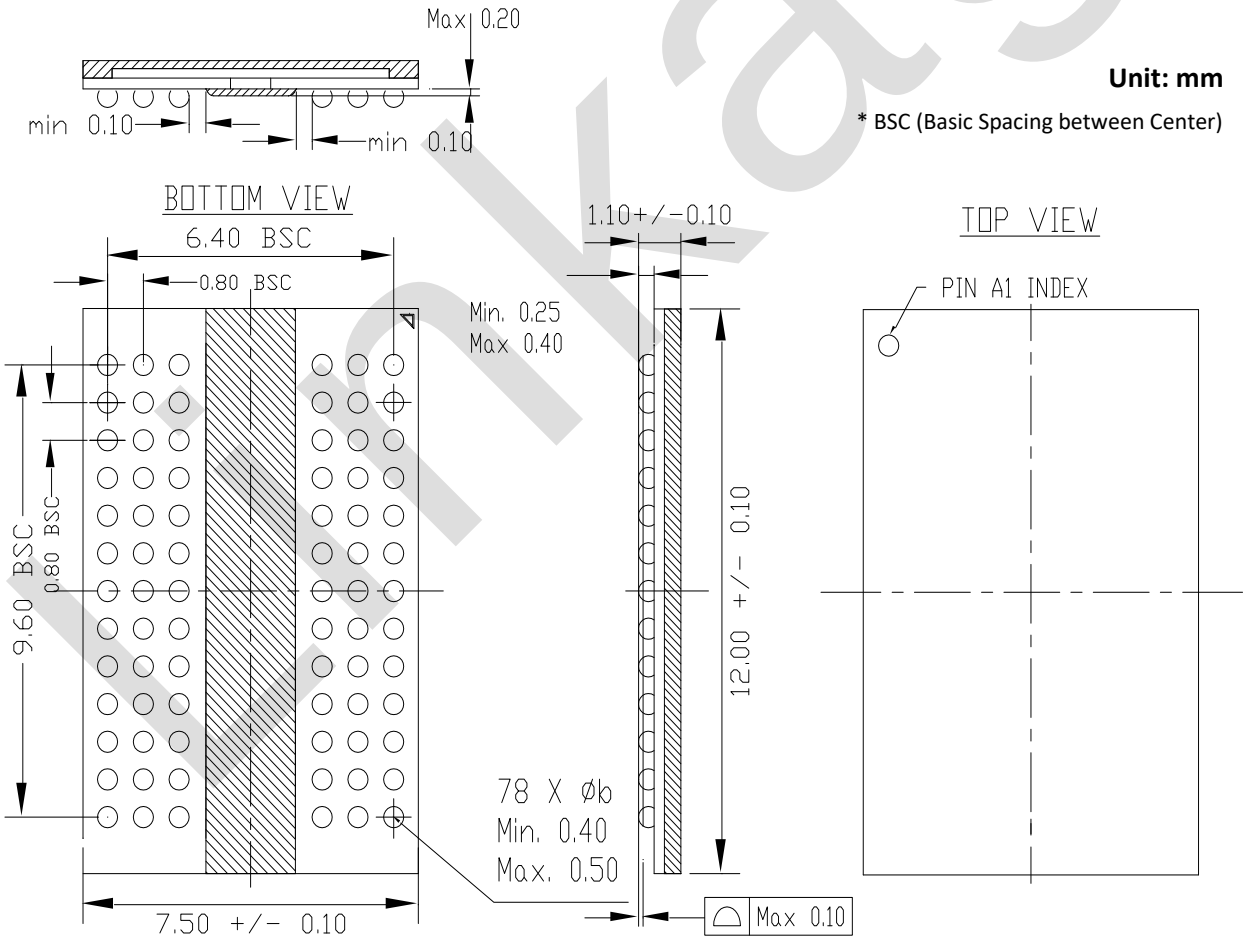
Ball Configuration – 78 Ball TFBGA Package (X8)

<TOP View>

See the balls through the package

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	$\overline{TDQS}$				DM/$\overline{DBI}$/TDQS	VSSQ	VSS	A
B	VPP	VDDQ	$\overline{DQS}$				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS				VDD	VSS	VDDQ	C
D	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	D
E	VSS	VDDQ	DQ6				DQ7	VDDQ	VSS	E
F	VDD	NC	ODT				CK	$\overline{CK}$	VDD	F
G	VSS	NC	CKE				$\overline{CS}$	NC	TEN	G
H	VDD	$\overline{WE}$/A14	$\overline{ACT}$				$\overline{CAS}$/A15	$\overline{RAS}$/A16	VSS	H
J	VREFCA	BG0	A10/AP				A12/$\overline{BC}$	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	$\overline{RESET}$	A6	A0				A1	A5	$\overline{ALERT}$	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				NC	A13	VDD	N
	1	2	3	4	5	6	7	8	9	

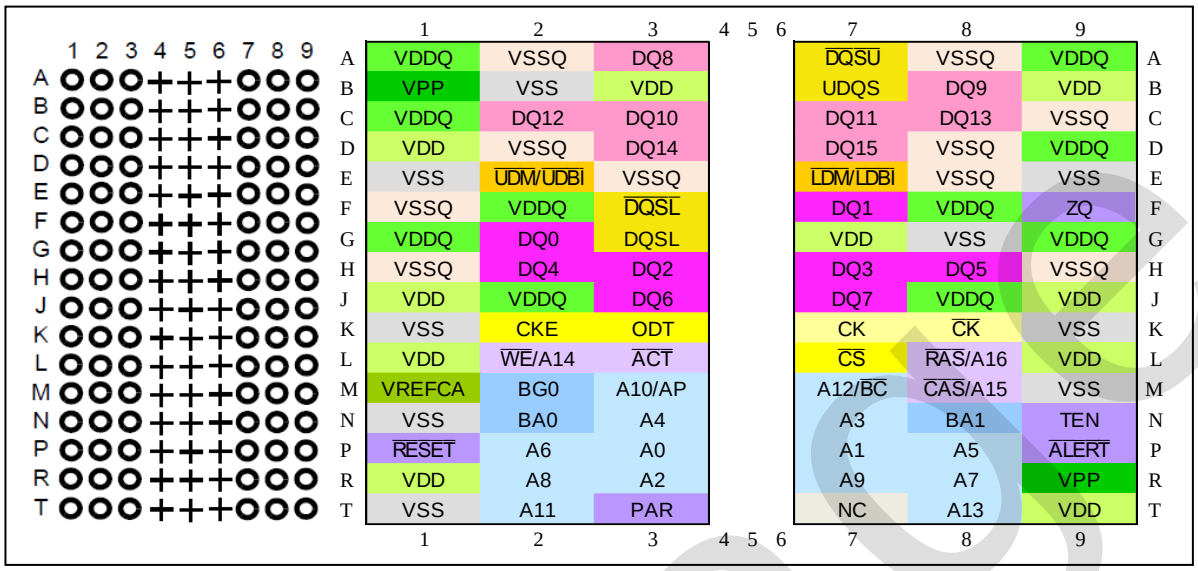
Package Outline Drawing



Ball Configuration – 96 Ball TFBGA Package (X16)

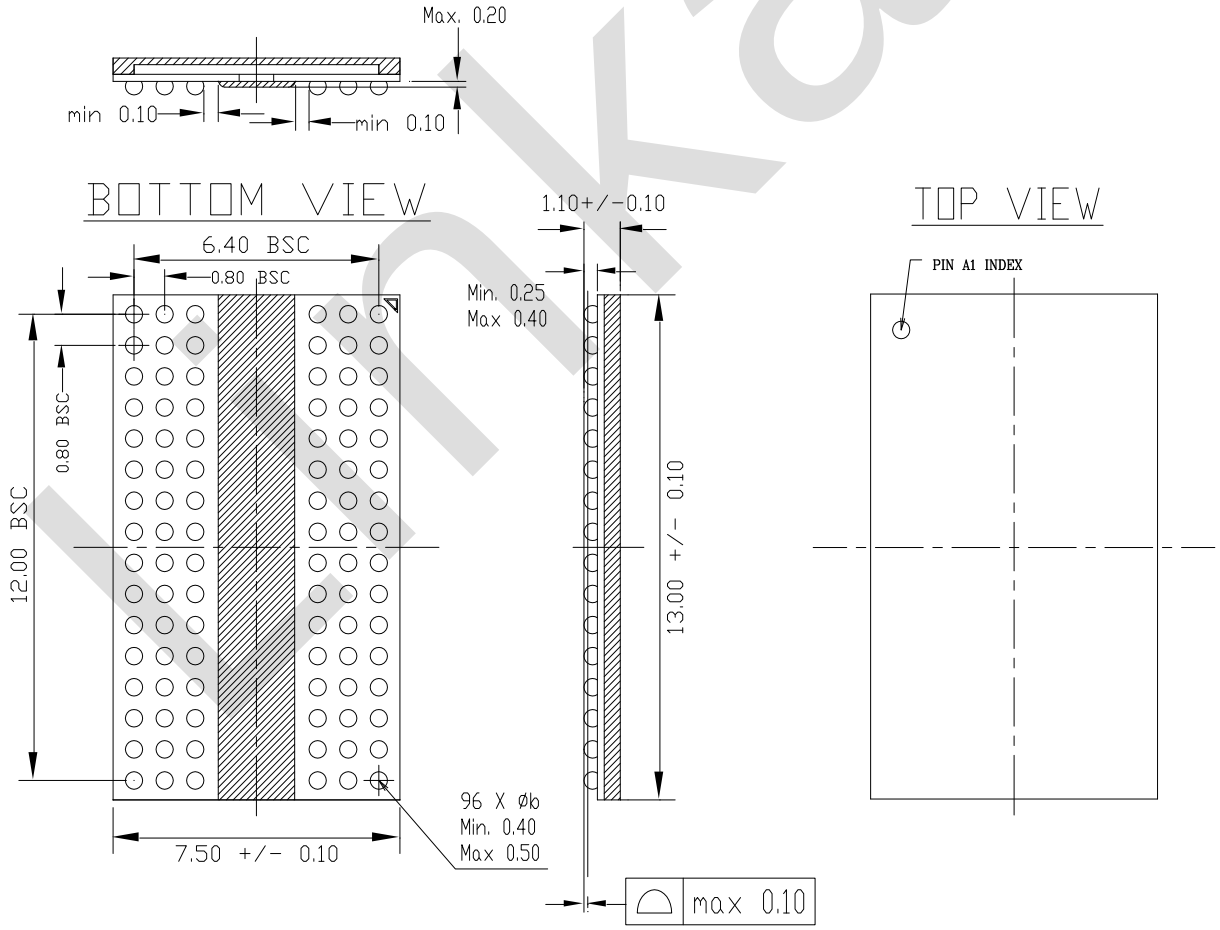
<TOP View>

See the balls through the package



	1	2	3	4 5 6	7	8	9	
A	VDDQ	VSSQ	DQ8		DQSU	VSSQ	VDDQ	A
B	VPP	VSS	VDD		UDQS	DQ9	VDD	B
C	VDDQ	DQ12	DQ10		DQ11	DQ13	VSSQ	C
D	VDD	VSSQ	DQ14		DQ15	VSSQ	VDDQ	D
E	VSS	UDM/UDBI	VSSQ		LDM/LDBI	VSSQ	VSS	E
F	VSSQ	VDDQ	DQSL		DQ1	VDDQ	ZQ	F
G	VDDQ	DQ0	DQSL		VDD	VSS	VDDQ	G
H	VSSQ	DQ4	DQ2		DQ3	DQ5	VSSQ	H
J	VDD	VDDQ	DQ6		DQ7	VDDQ	VDD	J
K	VSS	CKE	ODT		CK	CK	VSS	K
L	VDD	WE/A14	ACT		CS	RAS/A16	VDD	L
M	VREFCA	BG0	A10/AP		A12/BC	CAS/A15	VSS	M
N	VSS	BA0	A4		A3	BA1	TEN	N
P	RESET	A6	A0		A1	A5	ALERT	P
R	VDD	A8	A2		A9	A7	VPP	R
T	VSS	A11	PAR		NC	A13	VDD	T
	1	2	3	4 5 6	7	8	9	

Packge Outline Drawing



Ball Descriptions

Symbol	Type	Description
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE high activates, and CKE low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When ODT is enabled, on-die termination (RTT) is applied only to each DQ, DQS, $\overline{DQS}$, $\overline{DM}$/$\overline{DBI}$/TDQS, and $\overline{TDQS}$ signal for x4, x8 configurations (when the TDQS function is enabled via mode register). For the x16 configuration, RTT is applied to each DQ, DQSU, $\overline{DQSU}$, DQSL, $\overline{DQSL}$, $\overline{UDM}$, and $\overline{LDM}$ signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
BA[1:0]	Input	**Bank Address Inputs:** Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MRS cycle.
BG[1:0]	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0.
$\overline{ACT}$	Input	**Command input:** $\overline{ACT}$ defines the Activation command being entered along with $\overline{CS}$. The input into $\overline{RAS}$/A16, $\overline{CAS}$/A15 and $\overline{WE}$/A14 will be considered as Row Address A16, A15 and A14
$\overline{RAS}$/A16 $\overline{CAS}$/A15 $\overline{WE}$/A14	Input	**Command Inputs:** $\overline{RAS}$/A16, $\overline{CAS}$/A15 and $\overline{WE}$/A14 (along with $\overline{CS}$) define the command being entered. Those pins have multi-function. For example, for activation with $\overline{ACT}$ Low, those are Addressing like A16,A15 and A14 but for non-activation command with $\overline{ACT}$ High, those are Command pins for Read, Write and other command defined in command truth table.
A10/AP	Input	**Auto precharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/$\overline{BC}$	Input	**Burst Chop:** Burst chop: A12/$\overline{BC}$ is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst-chopped).
For x4, A[16:0] For x8,x16 A[15:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/$\overline{BC}$, $\overline{WE}$/A14, $\overline{CAS}$/A15, $\overline{RAS}$/A16, have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb.

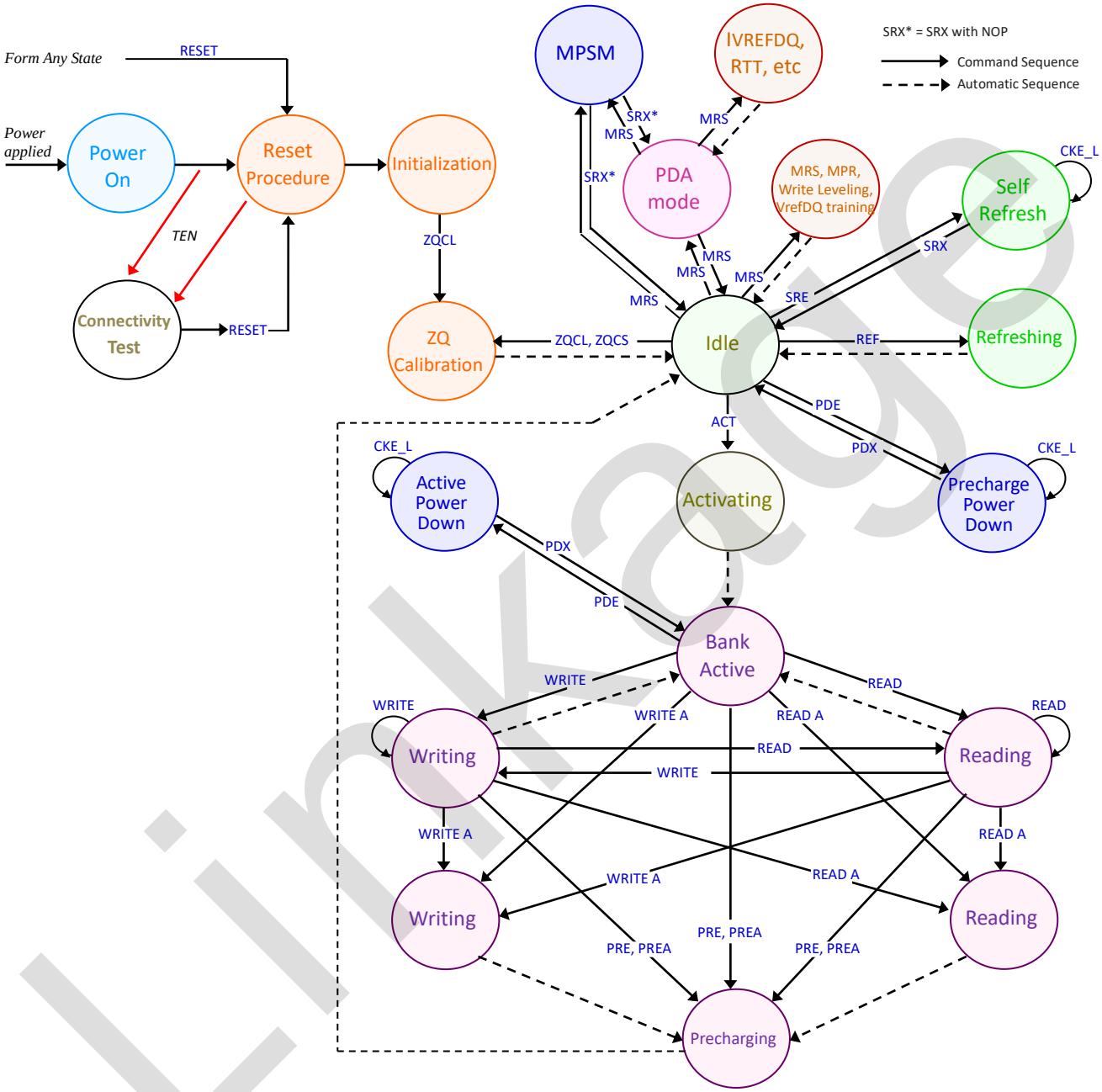
Symbol	Type	Description
PAR	Input	**Parity for command and address:** DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with $\overline{ACT}$,$\overline{RAS}$/A16,$\overline{CAS}$/A15,$\overline{WE}$/A14, A12/$\overline{BC}$,A10/AP, A17-A0, BA0-BA1, BG0-BG1 Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK and when $\overline{CS}$ is low.
DQ	Input/output	**Data input/output:** Bidirectional data bus. DQ represents DQ [3:0], DQ [7:0], and DQ [15:0] for the x4, x8, and x16 configurations, respectively. If Write CRC is enabled via Mode register, then the Write CRC code is added at the end of Data Burst. Either anyone or all DQ0, DQ1, DQ2, and DQ3 is used as monitoring of internal Vref level during test via Mode Register Setting MR4 A4=High, training times change when enabled. During this mode, RTT value should be set to Hi-Z. This measurement is for verification purposes and is NOT an external voltage supply pin.
DQS/$\overline{DQS}$ DQSL/$\overline{DQSL}$ DQSU/$\overline{DQSU}$	Input/output	**Data Strobe:** Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For the x16, DQSL corresponds to the data on DQ [7:0]; DQSU corresponds to the data on DQ [15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ [3:0] and DQ [7:0] respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
TDQS/$\overline{TDQS}$	Output	**Termination Data Strobe:** TDQS/$\overline{TDQS}$ is applicable for X8 DRAMs only. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same R_{TT} termination resistance function on TDQS/$\overline{TDQS}$ that is applied to DQS/$\overline{DQS}$. When the TDQS function is disabled via the mode register, the $\overline{DM}$/$\overline{DBI}$/TDQS pin will provide the data mask ($\overline{DM}$) function or Data Bus Inversion ($\overline{DBI}$) depending on MR5, and the $\overline{TDQS}$ pin is not used.
$\overline{DM}$ $\overline{LDM}$, $\overline{UDM}$	Input	**Input data mask:** $\overline{DM}$ is an input mask signal for write data. Input data is masked when $\overline{DM}$ is sampled LOW coincident with that input data during a write access. $\overline{DM}$ is sampled on both edges of DQS. $\overline{DM}$ is muxed with $\overline{DBI}$ function by Mode Register A [12:10] setting in MR5. For x8 device, the function of $\overline{DM}$ or TDQS is enabled by Mode Register A11 setting in MR1. $\overline{DBI}$ is an input/output identifying whether to store/output the true or inverted data. If $\overline{DBI}$ is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if $\overline{DBI}$ is HIGH. DM is not supported in X4.
$\overline{DBI}$ $\overline{UDBI}$, $\overline{LDBI}$	Input/output	**DBI input/output:** Data bus inversion. $\overline{DBI}$ is an input/output signal used for data bus inversion in the x8 configuration. $\overline{UDBI}$ and $\overline{LDBI}$ are used in the x16 configuration; $\overline{UDBI}$ is associated with DQ [15:8], and $\overline{LDBI}$ is associated with DQ [7:0]. The DBI feature is not supported on x4 configurations. $\overline{DBI}$ can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode register settings. See Data Bus Inversion (DBI).
$\overline{ALERT}$	Output	**Alert output:** It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then $\overline{ALERT}$ goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then $\overline{ALERT}$ goes LOW for relatively long period until ongoing DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, open-drain $\overline{ALERT}$ Pin must be bounded to VDD on board.
TEN	Input	**Connectivity test mode:** Connectivity Test Mode is active when TEN is HIGH, and inactive when TEN is LOW. TEN must be LOW during normal operation. TEN is a CMOS rail-to-rail signal with AC HIGH and LOW at 80% and 20% of VDD (960mV for DC HIGH and 240mV for DC LOW). Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
ZQ	Reference	**Reference pin for ZQ calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to VSSQ.
$\overline{RESET}$	Input	**Active Low Asynchronous Reset:** Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 0.96V for DC high and 0.24V for DC low.

Symbol	Type	Description
VPP	Supply	**DRAM activating power supply:** 2.5V (2.375V min , 2.75V max)
VDD	Supply	**Power Supply:** 1.2V ± 0.06V
VDDQ	Supply	**DQ Power Supply:** 1.2V ± 0.06V
VSS	Supply	**Ground**
VSSQ	Supply	**DQ Ground**
VREFCA	Supply	**Reference voltage for CA**
NC	-	**No Connect:** No internal electrical connection is present.
NF	-	**No function:** May have internal connection present, but has no function.
RFU	-	Reserved for future use.

NOTE Input only pins (BG0-BG1, BA0-BA1, A0-A17, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14, $\overline{CS}$, CKE, ODT, and $\overline{RESET}$) do not supply termination.

Functional Description

Simplified State Diagram



Abbr.	Function	Abbr.	Function	Abbr.	Function
ACT	Active	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh entry
RESET	Start RESET Procedure	Write A	WRA, WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh exit
ZQCS	ZQ Calibration Short	TEN	Boundary Scan Mode Enable	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	REF	Refresh, Fine granularity Refresh	MRS	Mode Register Set

Basic Functionality

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM. The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A15 select the row; refer to Addressing section for more details. The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

RESET and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values for the following MR settings are defined:

Default MR settings for power-up and reset initialization

MR functions	MR bits	Value
Gear-down mode	MR3 A[3]=0	1/2 Rate
Per DRAM Addressability	MR3 A[4]=0	Disable
Max Power Saving Mode	MR4 A[1]=0	Disable
$\overline{CS}$ to Command/Address Latency	MR4 A[8:6]=000	Disable
CA Parity Latency Mode	MR5 A[2:0]=000	Disable
Hard Post Package Repair Mode	MR4 A[13]=0	Disable
Soft Post Package Repair Mode	MR4 A[5]=0	Disable

Power-Up and Initialization Sequence

The following sequence (Step 1-15) is required for power-up and initialization:

1) Apply power ($\overline{RESET}$ and TEN are recommended to be maintained below 0.2 × VDD; all other inputs may be undefined). $\overline{RESET}$ needs to be maintained below 0.2 x VDD for minimum 200µs with stable power and TEN needs to be maintained below 0.2 x VDD for minimum 700µs with stable power. CKE is pulled "LOW" any time before $\overline{RESET}$ is being deasserted (MIN time 10ns). The power voltage ramp time between 300mV to VDD min must be no greater than 200ms, and during the ramp, VDD ≥ VDDQ and (VDD-VDDQ) < 0.3Volts. VPP must ramp at the same time or earlier than VDD, and VPP must be equal to or higher than VDD at all times.

   During power-up, either of the following conditions may exist and must be met:

   • Condition A
   – VDD and VDDQ are driven from a single-power converter output, AND
   – The voltage levels on all balls other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
   – VTT is limited to 0.76V MAX when the power ramp is finished, AND
   – VREFCA tracks VDD/2.

   • Condition B
   – Apply VDD without any slope reversal before or at the same time as VDDQ.
   – Apply VDDQ without any slope reversal before or at the same time as VTT and VREFCA.
   – Apply VPP without any slope reversal before or at the same time as VDD.
   – The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2) After $\overline{RESET}$ is de-asserted, wait for another 500µs until CKE becomes active.
   During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.

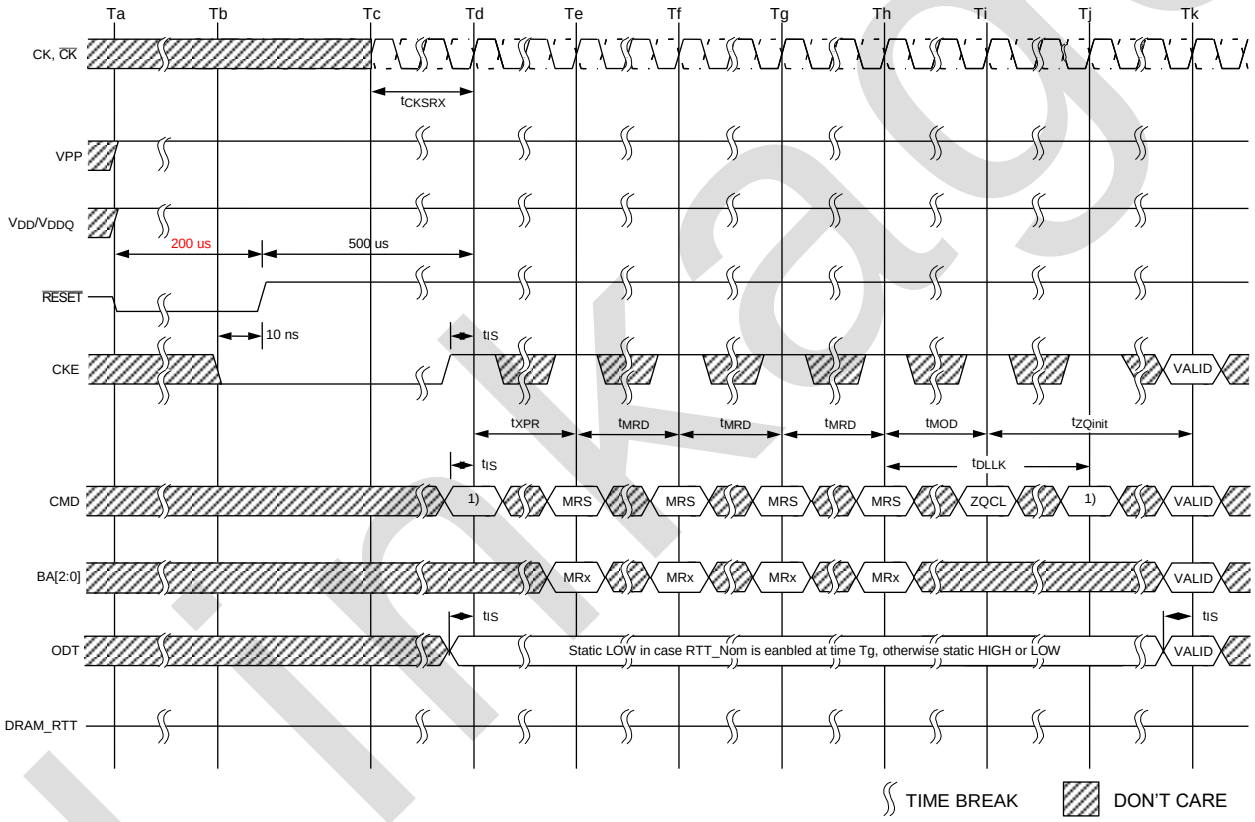
3) Clocks (CK, $\overline{CK}$) need to be started and stabilized for at least 10ns or 5 tCK (whichever is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a DESELECT command must be registered (with tIS setup time to clock) at clock edge Td. Once the CKE is registered "HIGH" after RESET, CKE needs to be continuously registered "HIGH" until the initialization sequence is finished, including expiration of tDLLK and tZQINIT.

4) The DDR4 SDRAM keeps its ODT in High-Impedance state as long as $\overline{RESET}$ is asserted. Further, the SDRAM keeps its ODT in High-Impedance state after $\overline{RESET}$ deassertion until CKE is registered HIGH. The ODT input signal may be in an undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power-up initialization sequence is

finished, including the expiration of tDLLK and tZQINIT.

5) After CKE is registered HIGH, wait a minimum of RESET CKE EXIT time, tXPR, before issuing the first MRS command to load mode register (tXPR = MAX (tXS; 5 × tCK).
6) Issue MRS command to load MR3 with all application settings, wait tMRD.
7) Issue MRS command to load MR6 with all application settings, wait tMRD.
8) Issue MRS command to load MR5 with all application settings, wait tMRD.
9) Issue MRS command to load MR4 with all application settings, wait tMRD.
10) Issue MRS command to load MR2 with all application settings, wait tMRD.
11) Issue MRS command to load MR1 with all application settings, wait tMRD.
12) Issue MRS command to load MR0 with all application settings, wait tMOD.
13) Issue a ZQCL command to starting ZQ calibration.
14) Wait for both tDLLK and tZQINIT completed.
15) The DDR4 SDRAM is now ready for read/write training (include Vref training and Write leveling).

RESET and Initialization Sequence at Power-On Ramping



NOTE 1 From the time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
NOTE 2 MRS commands must be issued to all mode registers that have defined settings.

VDD Slew rate at Power-up Initialization Sequence

VDD Slew Rate

Symbol	Min	Max	Units	NOTE
VDD_sl	0.004	600	V/ms	1,2
VDD_ona		200	ms	3

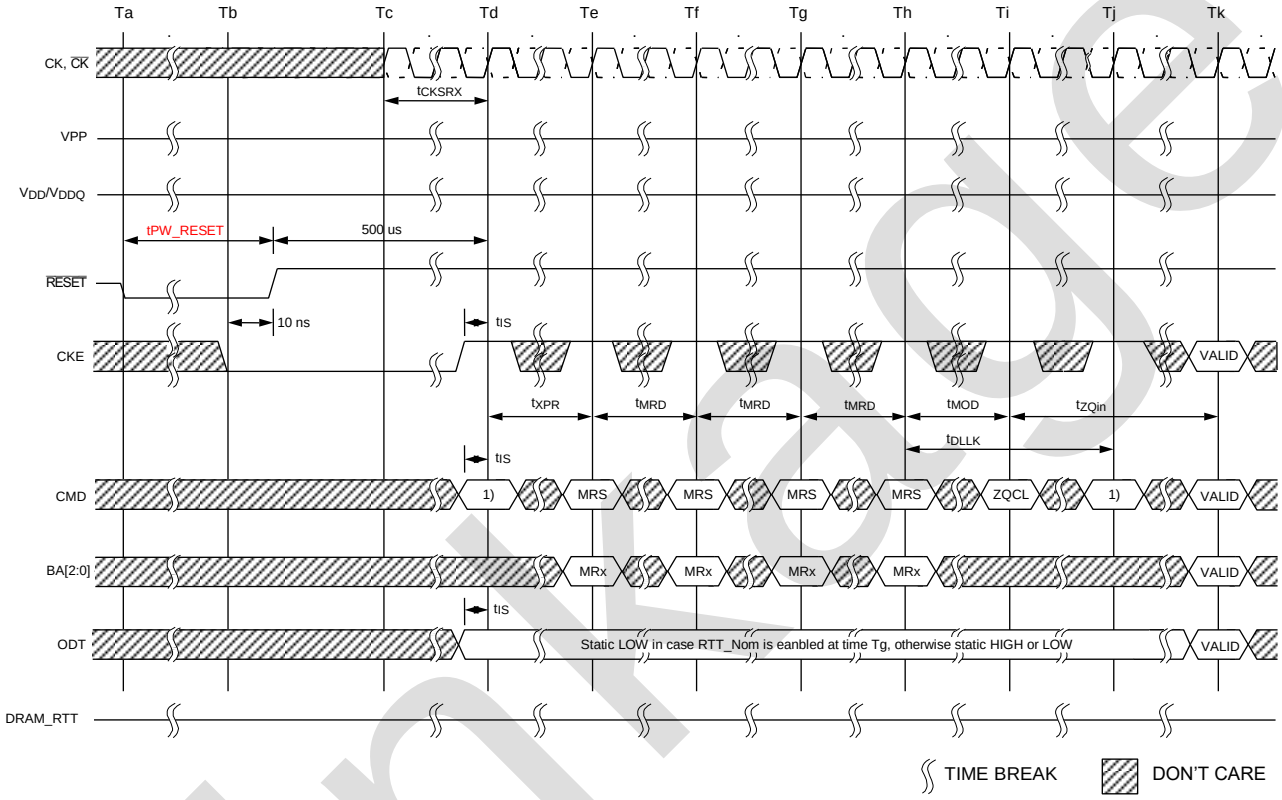
NOTE 1 Measurement made between 300mV and 80% VDD minimum.
NOTE 2 20 MHz bandlimited measurement
NOTE 3 Maximum time to ramp VDD from 300 mV to VDD minimum.

RESET Initialization with Stable Power Sequence

The following sequence is required for $\overline{\text{RESET}}$ at no power interruption initialization:

1. Assert $\overline{\text{RESET}}$ below 0.2 × VDD anytime when reset is needed (all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum tPW_RESET. CKE is pulled LOW before $\overline{\text{RESET}}$ being de-asserted (MIN time 10ns).
2. Follow Steps 2 to 10 in the Reset and Initialization Sequence at Power-on Ramping procedure.
3. The reset sequence is now completed, DDR4 SDRAM is ready for Read/Write training (include Vref training and Write leveling)

RESET Procedure at Power Stable



NOTE 1 From the time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
NOTE 2 MRS commands must be issued to all mode registers that have defined settings.

Register Definition

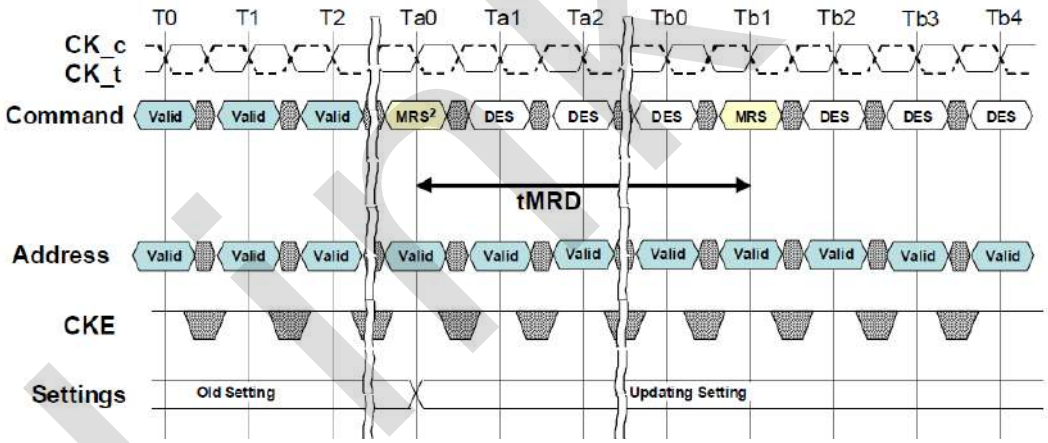
Programming the mode registers

For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR#) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i.e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. MRS Commands can be issued only when DRAM is at idle state. The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands.

tMRD Timing

Some of the Mode Register setting affect to address/command/control input functionality. These case, next MRS command can be allowed when the function updating by current MRS command completed.

The MRS commands which do not apply tMRD timing to next MRS command are listed in note 2 of the following figure. These MRS command input cases have unique MR setting procedure, so refer to individual function description.



NOTE 1 This timing diagram depicts C/A Parity Mode "Disabled" case.

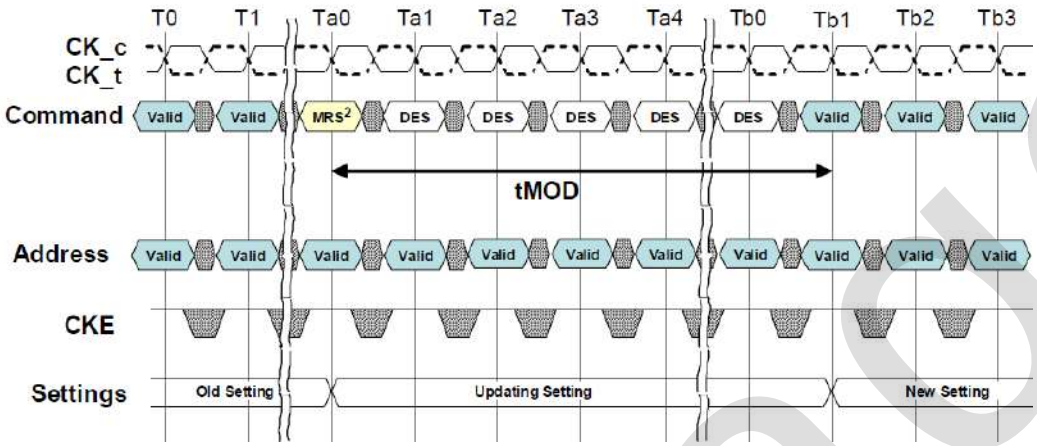
NOTE 2 tMRD applies to all MRS commands with the following exceptions:

- Geardown Mode
- C/A Parity Latency Mode
- CS to Command/Address Latency Mode
- Per DRAM Addressability Mode
- VrefDQ training value, VrefDQ training mode, and VrefDQ Training Range

tMOD Timing

The MRS command to nonMRS command delay, tMOD, is required for the DRAM to update features, except DLL RESET, and is the minimum time required from an MRS command to a nonMRS command, excluding DES.

Some of the mode register setting cases, function updating takes longer than tMOD. The MRS commands which do not apply tMOD timing to next valid command excluding DES is listed in note 2 of the following figure. These MRS command input cases have unique MR setting procedure, so refer to individual function description.



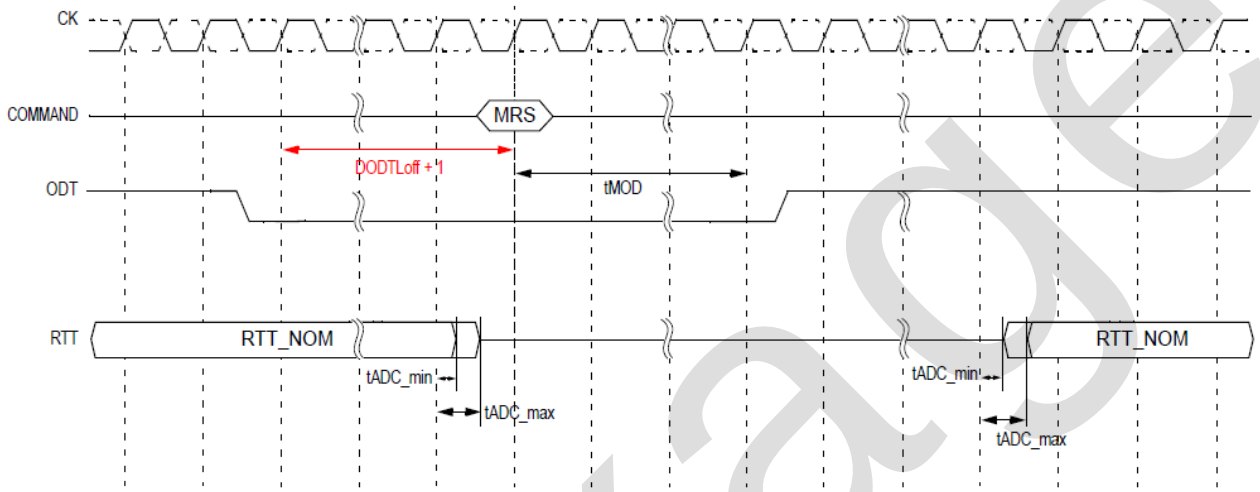
NOTE 1 This timing diagram depicts C/A Parity Mode "Disabled" case.

NOTE 2 List of MRS commands exception that do not apply to tMOD.

- DLL Enable, DLL Reset
- VrefDQ training value, internal Vref monitor, VrefDQ training mode, and VrefDQ Training Range
- Geardown Mode
- Per DRAM Addressability Mode
- Maximum Power Saving Mode
- CA Parity Mode

ODT Status at MRS affecting ODT turn-on/off timing

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. For MRS command, If RTT_Nom function is intended to change (enable to disable and vice versa) or already enabled in DRAM MR, ODT signal must be registered Low ensuring RTT_NOM is in an off state prior to MRS command affecting RTT_NOM turn-on and off timing. Refer to note2 of the following figure for this type of MRS. The ODT signal may be registered high after tMOD has expired. ODT signal is a don't care during MRS command if DRAM RTT_Nom function is disabled in the mode register prior and after an MRS command.



NOTE 1 This timing diagram shows CA Parity Latency mode is "Disable" case.

NOTE 2 When an MRS command mentioned in this note affects RTT_NOM turn on timings, RTT_NOM turn off timings and RTT_NOM value, this means the MR register value changes. The ODT signal should set to be low for at least DODTLoff +1 clock before their affecting MRS command is issued and remain low until tMOD expires. The following MR registers affects RTT_NOM turn on timings, RTT_NOM turn off timings and RTT_NOM value and it requires ODT to be low when an MRS command change the MR register value. If there are no change the MR register value that correspond to commands mentioned in this note, then ODT signal is not require to be low.

- DLL control for precharge power down
- Additive latency and CAS read latency
- DLL enable and disable
- CAS write latency
- CA Parity mode
- Gear Down mode
- RTT_NOM

Mode Register

MR0

Address	Operating Mode	Description
BG[1]	RFU	0 = must be programmed to 0 during MRS
BG[0], BA[1:0]	MR Select	BG0 / BA1 / BA0 / MR Select **0 / 0 / 0 / MR0** 0 / 0 / 1 / MR1 0 / 1 / 0 / MR2 0 / 1 / 1 / MR3 1 / 0 / 0 / MR4 1 / 0 / 1 / MR5 1 / 1 / 0 / MR6 1 / 1 / 1 / RCW[1]
A[17]	RFU	0 = must be programmed to 0 during MRS
A[13][5], A[11:9]	WR and RTP[2,3]	See table: Write Recovery and Read to Precharge
A[8]	DLL Reset	0 = No 1 = Yes
A[7]	TM	0 = Normal 1 = Test
A[12, 6:4, 2]	CAS Latency[4]	See Table: CAS Latency
A[3]	Read Burst Type	0 = Sequential 1 = Interleave
A[1:0]	Burst Length	00 = 8 (Fixed) Abbreviated BL8 01 = BC4 or 8 (on the fly) Abbreviated BC4OTF or BL8OTF 10 = BC4 (Fixed) Abbreviated BC4 11 = Reserved

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 2 WR (write recovery for autoprecharge) min in clock cycles is calculated by following rounding algorithm. The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

NOTE 3 The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.

NOTE 4 The table only shows the encodings for a given CAS Latency. For actual supported CAS Latency, please refer to speed bin tables for each frequency. CAS Latency controlled by A12 is optional for 4Gb device.

NOTE 5 A13 for WR and RTP setting is optional for 4Gb.

Write Recovery and Read to Precharge (cycles)

A13	A11	A10	A9	WR	RTP
0	0	0	0	10	5
0	0	0	1	12	6
0	0	1	0	14	7
0	0	1	1	16	8
0	1	0	0	18	9
0	1	0	1	20	10
0	1	1	0	24	12
0	1	1	1	22	11
1	0	0	0	26	13
1	0	0	1	RFU	RFU
1	0	1	0	RFU	RFU
1	0	1	1	RFU	RFU
1	1	0	0	RFU	RFU
1	1	0	1	RFU	RFU
1	1	1	0	RFU	RFU
1	1	1	1	RFU	RFU

CAS Latency

A12	A6	A5	A4	A2	CAS Latency
0	0	0	0	0	Reserved
0	0	0	0	1	Reserved
0	0	0	1	0	**11**
0	0	0	1	1	Reserved
0	0	1	0	0	**13**
0	0	1	0	1	Reserved
0	0	1	1	0	**15**
0	0	1	1	1	Reserved
0	1	0	0	0	**18**(1)
0	1	0	0	1	**20**(1)
0	1	0	1	0	**22**
0	1	0	1	1	Reserved
0	1	1	0	0	Reserved
0	1	1	0	1	**17**
0	1	1	1	0	**19**
0	1	1	1	1	**21**
1	0	0	0	0	**25**(1)
1	0	0	0	1	**26**(1)
1	0	0	1	0	Reserved
1	0	0	1	1	Reserved
1	0	1	0	0	Reserved
1	0	1	0	1	Reserved
1	0	1	1	0	Reserved
1	0	1	1	1	Reserved
1	1	0	0	0	Reserved

Note 1: this CL setting is related to read DBI usage only and please check “Speed bin” section and have a proper corresponding option to use.

MR1

<table>
<tr><th>Address</th><th>Operating Mode</th><th>Description</th></tr>
<tr><td>BG[1]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>BG[0], BA[1:0]</td><td>MR Select</td><td>
<table>
<tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MR6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>RCW[3]</td></tr>
</table>
</td></tr>
<tr><td>A[17]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>A[13], A[6:5]</td><td>Rx CTLE control[4]</td><td>000 = Vendor Optimized Setting (default)
001 = Vendor defined
010 = Vendor defined
011 = Vendor defined
100 = Vendor defined
101 = Vendor defined
110 = Vendor defined
111 = Vendor defined</td></tr>
<tr><td>A[12]</td><td>Qoff[1]</td><td>0 = Output buffer enable
1 = Output buffer disable</td></tr>
<tr><td>A[11]</td><td>TDQS enable</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[10:8]</td><td>RTT_NOM</td><td>See Table: RTT_NOM</td></tr>
<tr><td>A[7]</td><td>Write Leveling Enable</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[4:3]</td><td>Additive Latency</td><td>00 = 0 (AL disabled)
01 = CL-1
10 = CL-2
11 = Reserved</td></tr>
<tr><td>A[2:1]</td><td>Output Driver Impedance Control</td><td>See Table: Output Driver Impedance Control</td></tr>
<tr><td>A[0]</td><td>DLL Enable</td><td>0 = Disable[2]
1 = Enable</td></tr>
</table>

NOTE 1 Outputs disabled - DQs, DQSs, $\overline{\text{DQS}}$s.

NOTE 2 States reversed to “0 as Disable” with respect to DDR4.

NOTE 3 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn’t respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 4 For this function, please confirm with NTC.

RTT_NOM

A10	A9	A8	RTT_NOM
0	0	0	Disabled
0	0	1	RZQ/4 (60 Ω)
0	1	0	RZQ/2 (120 Ω)
0	1	1	RZQ/6 (40 Ω)
1	0	0	RZQ/1 (240 Ω)
1	0	1	RZQ/5 (48 Ω)
1	1	0	RZQ/3 (80 Ω)
1	1	1	RZQ/7 (34 Ω)

Output Driver Impedance Control

A2	A1	ODI
0	0	RZQ/7(34 ohm)
0	1	RZQ/5(48 ohm)
1	0	RFU
1	1	RFU

MR2

<table>
<tr><th>Address</th><th>Operating Mode</th><th>Description</th></tr>
<tr><td>BG[1]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>BG[0], BA[1:0]</td><td>MR Select</td><td>
<table>
<tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MR6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>RCW[1]</td></tr>
</table>
</td></tr>
<tr><td>A[17]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>A[13]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>A[12]</td><td>Write_CRC</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[11:9]</td><td>RTT_WR</td><td>See Table: RTT_WR</td></tr>
<tr><td>A[8]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>A[7:6]</td><td>Low Power Auto Self Refresh (LPASR)</td><td>00 = Manual Mode (Normal Operating Temperature Range)
01 = Manual Mode (Reduced Operating Temperature Range)
10 = Manual Mode (Extended Operating Temperature Range)
11 = ASR Mode (Auto Self Refresh)</td></tr>
<tr><td>A[5:3]</td><td>CAS Write Latency(CWL)</td><td>See Table: CWL (CAS Write Latency)</td></tr>
<tr><td>A[2:0]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
</table>

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

RTT_WR

A11	A10	A9	RTT_WR
0	0	0	Dynamic ODT off
0	0	1	RZQ/2
0	1	0	RZQ/1
0	1	1	Hi-Z
1	0	0	RZQ/3
1	0	1	RFU
1	1	0	RFU
1	1	1	RFU

CAS Write Latency (CWL)

A5	A4	A3	CWL	Speed Grade in MT/s			
				1 tCK tWPRE		2 tCK tWPRE[1]	
				1st Set	2nd Set	1st Set	2nd Set
0	0	0	9	1600	-	-	-
0	0	1	10	1866	-	-	-
0	1	0	11	2133	1600	-	-
0	1	1	12	2400	1866	-	-
1	0	0	14	2666	2133	2400	-
1	0	1	16	-	2400	2666	2400
1	1	0	18	-	2666	2933/3200	2666
1	1	1	20	-	2933/3200	-	2933/3200

NOTE 1 The 2 tCK Write Preamble is valid for DDR4-2400/2666/2933/3200 Speed Grade. For the 2nd Set of 2 tCK Write Preamble, no additional CWL is needed.

MR3

<table>
<tr><th>Address</th><th>Operating Mode</th><th>Description</th></tr>
<tr><td>BG[1]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>BG[0], BA[1:0]</td><td>MR Select</td><td>
<table>
<tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MR6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>RCW[1]</td></tr>
</table>
</td></tr>
<tr><td>A[17]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>A[13]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>A[12:11]</td><td>MPR Read Format</td><td>00 = Serial
01 = Parallel
10 = Staggered
11 = Reserved</td></tr>
<tr><td>A[10:9]</td><td>Write CMD Latency
when CRC and DM are enabled</td><td>See Table:
Write Command Latency when CRC and DM are both enabled</td></tr>
<tr><td>A[8:6]</td><td>Fine Granularity Refresh Mode</td><td>See Table: Fine Granularity Refresh Mode</td></tr>
<tr><td>A[5]</td><td>Temperature sensor readout[2]</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[4]</td><td>Per DRAM Addressability</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[3]</td><td>Geardown Mode</td><td>0 = 1/2 Rate
1 = 1/4 Rate</td></tr>
<tr><td>A[2]</td><td>MPR Operation</td><td>0 = Normal
1 = Dataflow from/to MPR</td></tr>
<tr><td>A[1:0]</td><td>MPR Page Selection</td><td>00 = Page0
01 = Page1
10 = Page2
11 = Page3
See Table: MPR Data Format</td></tr>
</table>

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 2 Please confirm with NTC.

Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh Mode
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	RFU
1	0	0	RFU
1	0	1	Enable On-the-fly 1x/2x
1	1	0	Enable On-the-fly 1x/4x
1	1	1	RFU

MR3 A<10:9> Write Command Latency when CRC and DM are both enabled

A10	A9	CRC+DM Write CMD Latency	Operating Data Rate
0	0	4nCK	1600
0	1	5nCK	1866/2133/2400/2666
1	0	6nCK	2933/3200
1	1	RFU	RFU

NOTE 1 Write Command latency when CRC and DM are both enabled
NOTE 2 At less than or equal to 1600 then 4nCK; neither 5nCK nor 6nCK
NOTE 3 At greater than 1600 and less than or equal to 2666 then 5nCK; neither 4nCK nor 6nCK
NOTE 4 At greater than 2666 and less than or equal to 3200 then 6nCK; neither 4nCK nor 5nCK

MPR Data Format

MR3 MPR Page A[1:0]	Purpose	MPR Location BA[1:0]	MPR Bit Write Location [7:0]								Note
			7	6	5	4	3	2	1	0	
			Read Burst Order (serial mode)								
			UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7	
00 Page 0	Training Patterns	**00** = MPR0	0	1	0	1	0	1	0	1	1,2
		01 = MPR1	0	0	1	1	0	0	1	1	
		10 = MPR2	0	0	0	0	1	1	1	1	
		11 = MPR3	0	0	0	0	0	0	0	0	
01 Page 1	C/A Parity Error Log	**00** = MPR0	A7	A6	A5	A4	A3	A2	A1	A0	3,4,5,6
		01 = MPR1	$\overline{CAS}$/A15	$\overline{WE}$/A14	A13	A12	A11	A10	A9	A8	
		10 = MPR2	PAR	$\overline{ACT}$	BG1	BG0	BA1	BA0	A17[6]	$\overline{RAS}$/A16	
		11 = MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency[6]			-	-	-	
					MR5	MR5	MR5				
					A2	A1	A0				
10 Page 2	MRS Readout	**00** = MPR0	hPPR	sPPR	RTT_WR	Temperature Sensor Status[8]		CRC Write Enable	R_{TT}_WR		
			-	-	MR2	Refer to next table		MR2	MR2		
			-	-	A11			A12	A10	A9	
		01 = MPR1	Vref DQ range	Vref DQ training Value						Geardown Enable	
			MR6	MR6						MR3	
			A6	A5	A4	A3	A2	A1	A0	A3	
		10 = MPR2	CAS Latency					CAS Write Latency			
			MR0					MR2			
			A6	A5	A4	A2	A12	A5	A4	A3	
		11 = MPR3	R_{TT}_NOM			R_{TT}_PARK			Driver Impedance		
			MR1			MR5			MR1		
			A10	A9	A6	A8	A7	A6	A2	A1	
11 Page 3	Vendor use only[7]	**00** = MPR0	Don't care								7
		01 = MPR1	Don't care								
		10 = MPR2	Don't care								
		11 = MPR3	Don't care								

NOTE 1 MPRx using A7:A0 that A7 is mapped to location [7] and A0 is mapped to location [0].
NOTE 2 Training pattern be defined by MPR0-MPR3 which are default value of Page 0 read and write
NOTE 3 MPR used for C/A parity error log readout is enabled by setting A [2] in MR3
NOTE 4 For higher density of DRAM, where A [17] is not used, MPR2[1] should be treated as don't care.
NOTE 5 If a device is used in monolithic application, where C [2:0] are not used, then MPR3[2:0] should be treated as don't care.
NOTE 6 MPR3 bit 0~2 (CA parity latency) reflects the latest programmed CA parity latency values.
NOTE 7 MPR page3 is specifically assigned to DRAM. Actual encoding method is vendor specific.
NOTE 8 Please confirm with NTC.

Temperature Sensor Status

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range	MR3[5]
0	0	Sub 1x refresh (>tREFI)	**MR3 bit A5=1 (Temperature sensor readout = Enabled)** DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A [4:3]). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits. **MR3 bit A5=0 (Temperature sensor readout = Disabled)** DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0-bit A[4:3])
0	1	1x refresh rate (= tREFI)	
1	0	2x refresh rate (1/2 x tREFI)	
1	1	RFU	

MR4

<table>
<tr><th>Address</th><th>Operating Mode</th><th>Description</th></tr>
<tr><td>BG[1]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>BG[0], BA[1:0]</td><td>MR Select</td><td>
<table>
<tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MR6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>RCW[1]</td></tr>
</table>
</td></tr>
<tr><td>A[17]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>A[13]</td><td>hPPR</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[12]</td><td>Write Preamble</td><td>0 = 1 nCK
1 = 2 nCK</td></tr>
<tr><td>A[11]</td><td>Read Preamble</td><td>0 = 1 nCK
1 = 2 nCK</td></tr>
<tr><td>A[10]</td><td>Read Preamble Taring Mode</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[9]</td><td>Self Refresh Abort</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[8:6]</td><td>CS to CMD/ADDR Latency Mode (Cycles)</td><td>See Table: CS to CMD/ADDR Latency Mode Setting</td></tr>
<tr><td>A[5]</td><td>sPPR</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[4]</td><td>Internal Vref Monitor</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[3]</td><td>Temperature Controlled Refresh Mode</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[2]</td><td>Temperature Controlled Refresh Range</td><td>0 = Normal
1 = Extended</td></tr>
<tr><td>A[1]</td><td>Maximum Power Down Mode</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[0]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
</table>

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

CS to CMD / ADDR Latency Mode Setting

A8	A7	A6	CAL
0	0	0	Disabled
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	Reserved
1	1	1	Reserved

MR5

<table>
<tr><th>Address</th><th>Operating Mode</th><th>Description</th></tr>
<tr><td>BG[1]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>BG[0], BA[1:0]</td><td>MR Select</td><td>
<table>
<tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MR6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>RCW[1]</td></tr>
</table>
</td></tr>
<tr><td>A[17]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>A[13]</td><td>RFU</td><td>0 = must be programmed to 0 during MRS</td></tr>
<tr><td>A[12]</td><td>Read DBI</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[11]</td><td>Write DBI</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[10]</td><td>Data Mask</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[9]</td><td>CA Parity Persistent Error</td><td>0 = Disable
1 = Enable</td></tr>
<tr><td>A[8:6]</td><td>RTT_PARK</td><td>See Table: RTT_PARK</td></tr>
<tr><td>A[5]</td><td>ODT Input Buffer during Power Down Mode</td><td>0 = ODT input buffer is activated
1 = ODT input buffer is deactivated</td></tr>
<tr><td>A[4]</td><td>C/A Parity Error Status</td><td>0 = Clear
1 = Error</td></tr>
<tr><td>A[3]</td><td>CRC Error Clear</td><td>0 = Clear
1 = Error</td></tr>
<tr><td>A[2:0]</td><td>C/A Parity Latency Mode</td><td>See Table: C/A Parity Latency Mode</td></tr>
</table>

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 2 When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.

RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

C/A Parity Latency Mode

A2	A1	A0	CA Parity Latency	Speed Bin
0	0	0	Disabled	
0	0	1	4	1600/1866/2133
0	1	0	5	2400/2666
0	1	1	6	2933/3200
1	0	0	8	RFU
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

NOTE 1 Parity latency must be programmed according to timing parameters by speed grade table.

MR6

Address	Operating Mode	Description
BG[1]	RFU	0 = must be programmed to 0 during MRS
BG[0], BA[1:0]	MR Select	<table><tr><th>BG0</th><th>BA1</th><th>BA0</th><th>MR Select</th></tr><tr><td>0</td><td>0</td><td>0</td><td>MR0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>MR1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>MR2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>MR3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>MR4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>MR5</td></tr><tr><td>**1**</td><td>**1**</td><td>**0**</td><td>**MR6**</td></tr><tr><td>1</td><td>1</td><td>1</td><td>RCW[1]</td></tr></table>
A[17]	RFU	0 = must be programmed to 0 during MRS
A[13]	RFU	0 = must be programmed to 0 during MRS
A[12:10]	tCCD_L	See Table: tCCD_L & tDLLK
A[9:8]	RFU	0 = must be programmed to 0 during MRS
A[7]	VrefDQ Training Enable	0 = Disable (Normal Operation Mode) 1 = Enable(Training Mode)
A[6]	VrefDQ Training Range	0 = Range 1 1 = Range 2
A[5:0]	VrefDQ Training Value	See Table: VrefDQ Training Values

NOTE 1 Reserved for Register control word setting. DRAM ignores MR command with BG0, BA [1:0] =111 and doesn't respond.

tCCD_L & tDLLK

A12	A11	A10	tCCD_L.min(nCK)	tDLLK.min(nCK)	Note
0	0	0	Reserved	-	-
0	0	1	5	597	1600Mbps ≦ Data rate ≦ 1866Mbps (1600/1866Mbps)
0	1	0	6	768	1866Mbps < Data rate ≦ 2400Mbps (2133/2400Mbps)
0	1	1	7	1024	2400Mbps < Data rate ≦ 2666Mbps (2666 Mbps)
1	0	0	8		2666Mbps < Data rate ≦ 3200Mbps (2933/3200 Mbps)
1	0	1	Reserved	-	-
1	1	0			-
1	1	1			-

NOTE 1 tCCD_L/tDLLK should be programmed according to the value defined in AC parameter table per operating frequency.

VrefDQ Training Values

MR6 [5:0]	Range 1 MR6 A6=0	Range 2 MR6 A6=1	MR6 [5:0]	Range 1 MR6 A6=0	Range 2 MR6 A6=1	MR6 [5:0]	Range 1 MR6 A6=0	Range 2 MR6 A6=1	MR6 [5:0]	Range 1 MR6 A6=0	Range 2 MR6 A6=1
000000	60.00%	45.00%	001101	68.45%	53.45%	011010	76.90%	61.90%	100111	85.35%	70.35%
000001	60.65%	45.65%	001110	69.10%	54.10%	011011	77.55%	62.55%	101000	86.00%	71.00%
000010	61.30%	46.30%	001111	69.75%	54.75%	011100	78.20%	63.20%	101001	86.65%	71.65%
000011	61.95%	46.95%	010000	70.40%	55.40%	011101	78.85%	63.85%	101010	87.30%	72.30%
000100	62.60%	47.60%	010001	71.05%	56.05%	011110	79.50%	64.50%	101011	87.95%	72.95%
000101	63.25%	48.25%	010010	71.70%	56.70%	011111	80.15%	65.15%	101100	88.60%	73.60%
000110	63.90%	48.90%	010011	72.35%	57.35%	100000	80.80%	65.80%	101101	89.25%	74.25%
000111	64.55%	49.55%	010100	73.00%	58.00%	100001	81.45%	66.45%	101110	89.90%	74.90%
001000	65.20%	50.20%	010101	73.65%	58.65%	100010	82.10%	67.10%	101111	90.55%	75.55%
001001	65.85%	50.85%	010110	74.30%	59.30%	100011	82.75%	67.75%	110000	91.20%	76.20%
001010	66.50%	51.50%	010111	74.95%	59.95%	100100	83.40%	68.40%	110001	91.85%	76.85%
001011	67.15%	52.15%	011000	75.60%	60.60%	100101	84.05%	69.05%	110010	92.50%	77.50%
001100	67.80%	52.80%	011001	76.25%	61.25%	100110	84.70%	69.70%	110011 to 111111	Reserved	Reserved

MR7 DRAM: Ignore

The DDR4 SDRAM shall ignore any access to MR7 for all DDR4 SDRAM. Any bit setting within MR7 may not take any effect in the DDR4 SDRAM.

DDR4 SDRAM Command Description and Operation

Command Truth Table

Note 1,2,3 and 4 apply to the entire Command truth table.
Note 5 applies to all Read/Write commands.
BG = Bank Group Address; BA = Bank Address; RA =Row Address; CA = Column Address;$\overline{BC}$ = Burst Chop;
X = Don't Care; V = Valid H or L

Symbol	Function		CKE		$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$ /A16	$\overline{CAS}$ /A15	$\overline{WE}$ /A14	BG [1:0]	BA [1:0]	A12 /$\overline{BC}$	A [13,11]	A10 /AP	A [9:0]	Notes
			Prev.	Pres.												
MRS	Mode Register Set		H	H	L	H	L	L	L	BG		OP code				12
REF	REFRESH		H	H	L	H	L	L	H	V	V	V	V	V	V	
SRE	Self Refresh Entry		H	L	L	H	L	L	H	V	V	V	V	V	V	7,9
SRX	Self Refresh Exit		L	H	H	X	X	X	X	X	X	X	X	X	X	7,8,9,10
					L	H	H	H	H	V	V	V	V	V	V	
PRE	Single-Bank Precharge		H	H	L	H	L	H	L	BG	BA	V	V	L	V	
PREA	Precharge All Banks		H	H	L	H	L	H	L	V	V	V	V	H	V	
RFU	Reserved For Future Use		H	H	L	H	L	H	H	RFU						
ACT	Bank Active		H	H	L	L	Row Address(RA)			BG	BA	Row Address (RA)				
WR	WRITE	Fixed BL8 or BC4	H	H	L	H	H	L	L	BG	BA	V	V	L	CA	
WRS4		BC4,on the fly	H	H	L	H	H	L	L	BG	BA	L	V	L	CA	
WRS8		BL8,on the fly	H	H	L	H	H	L	L	BG	BA	H	V	L	CA	
WRA	WRITE with auto precharge	Fixed BL8 or BC4	H	H	L	H	H	L	L	BG	BA	V	V	H	CA	
WRAS4		BC4,on the fly	H	H	L	H	H	L	L	BG	BA	L	V	H	CA	
WRAS8		BL8,on the fly	H	H	L	H	H	L	L	BG	BA	H	V	H	CA	
RD	READ	Fixed BL8 or BC4	H	H	L	H	H	L	H	BG	BA	V	V	L	CA	
RDS4		BC4,on the fly	H	H	L	H	H	L	H	BG	BA	L	V	L	CA	
RDS8		BL8,on the fly	H	H	L	H	H	L	H	BG	BA	H	V	L	CA	
RDA	READ with auto precharge	Fixed BL8 or BC4	H	H	L	H	H	L	H	BG	BA	V	V	H	CA	
RDAS4		BC4,on the fly	H	H	L	H	H	L	H	BG	BA	L	V	H	CA	
RDAS8		BL8,on the fly	H	H	L	H	H	L	H	BG	BA	H	V	H	CA	
NOP	No Operation		H	H	L	H	H	H	H	V	V	V	V	V	V	10
DES	Device Deselected		H	H	H	X	X	X	X	X	X	X	X	X	X	
PDE	Power Down Entry		H	L	H	X	X	X	X	X	X	X	X	X	X	6
PDX	Power Down Exit		L	H	H	X	X	X	X	X	X	X	X	X	X	6
ZQCL	ZQ Calibration Long		H	H	L	H	H	H	L	V	V	V	V	H	V	
ZQCS	ZQ Calibration Short		H	H	L	H	H	H	L	V	V	V	V	L	V	

NOTE 1 All DDR4 SDRAM commands are defined by states of $\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependent. When $\overline{ACT}$ = H; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as command pins $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ respectively. When $\overline{ACT}$= L; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as address pins A16, A15, and A14 respectively.

NOTE 2 $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.

NOTE 3 Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.

NOTE 4 "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".

NOTE 5 Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.

NOTE 6 The Power Down Mode does not perform any refresh operation.

NOTE 7 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

NOTE 8 Controller guarantees self refresh exit to be synchronous.

NOTE 9 VPP and VREF(VrefCA) must be maintained during Self Refresh operation.

NOTE 10 The No Operation command should be used in cases when the DDR4 SDRAM is in Gear Down Mode and Max Power Saving Mode Exit

NOTE 11 Refer to the CKE Truth Table for more detail with CKE transition.

NOTE 12 During a MRS command A17 is Reserved for Future Use and is device density and configuration dependent.

CKE Truth Table

Current State[2]	CKE		Command (N)[3]	Action(N)[3]	Notes
	Previous Cycle[1] (N-1)	Present Cycle[1] (N)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$		
Power Down	L	L	X	Maintain power down	14, 15
	L	H	DESELECT	Power down exit	11, 14
Self Refresh	L	L	X	Maintain self refresh	15, 16
	L	H	DESELECT	Self refresh exit	8, 12, 16
Bank(s) Active	H	L	DESELECT	Active power down entry	11, 13, 14
Reading	H	L	DESELECT	Power down entry	11, 13, 14, 17
Writing	H	L	DESELECT	Power down entry	11, 13, 14, 17
Precharging	H	L	DESELECT	Power down entry	11, 13, 14, 17
Refreshing	H	L	DESELECT	Precharge power down entry	11
All Banks idle	H	L	DESELECT	Precharge power down entry	11,13, 14, 18
	H	L	REFRESH	Self refresh	9, 13, 18
For more details with all signals See “Command Truth Table”.					10

NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.

NOTE 2 Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge N.

NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.

NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

NOTE 6 During any CKE transition (registration of CKE H->L or CKE L->H), the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).

NOTE 7 DESELECT and NOP are defined in the Command Truth Table.

NOTE 8 On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

NOTE 9 Self-Refresh mode can only be entered from the All Banks Idle state.

NOTE 10 Must be a legal command as defined in the Command Truth Table.

NOTE 11 Valid commands for Power-Down Entry and Exit are DESELECT only.

NOTE 12 Valid commands for Self-Refresh Exit are DESELECT only except for Gear Down mode and Max Power Saving exit. NOP is allowed for these 2 modes.

NOTE 13 Self-Refresh cannot be entered during Read or Write operations. For a detailed list of restrictions, see “Self-Refresh Operation” and “Power-Down Modes”.

NOTE 14 The Power-Down does not perform any refresh operations.

NOTE 15 “X” means “don’t care “(including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

NOTE 16 VPP and VREF(VrefCA) must be maintained during Self-Refresh operation.

NOTE 17 If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.

NOTE 18 ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, etc).

Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in the following: Burst Type and Burst Order table. The burst type is selected via A3 of Mode Register MR0. The burst length is defined by A0-A1 of Mode Register MR0. Burst length options include fixed BC4, fixed BL8, and on-the-fly (OTF), which allows BC4 or BL8 to be selected coincident with the registration of a READ or WRITE command via A12/$\overline{BC}$.

Burst Length	READ/ WRITE	Starting Column Address			Burst Type (Decimal)																Notes
					Sequential								Interleaved								
		A2	A1	A0	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
BC4	READ	0	0	0	0	1	2	3	T	T	T	T	0	1	2	3	T	T	T	T	1,2,3
		0	0	1	1	2	3	0	T	T	T	T	1	0	3	2	T	T	T	T	1,2,3
		0	1	0	2	3	0	1	T	T	T	T	2	3	0	1	T	T	T	T	1,2,3
		0	1	1	3	0	1	2	T	T	T	T	3	2	1	0	T	T	T	T	1,2,3
		1	0	0	4	5	6	7	T	T	T	T	4	5	6	7	T	T	T	T	1,2,3
		1	0	1	5	6	7	4	T	T	T	T	5	4	7	6	T	T	T	T	1,2,3
		1	1	0	6	7	4	5	T	T	T	T	6	7	4	5	T	T	T	T	1,2,3
		1	1	1	7	4	5	6	T	T	T	T	7	6	5	4	T	T	T	T	1,2,3
	WRITE	0	V	V	0	1	2	3	X	X	X	X	0	1	2	3	X	X	X	X	1,2,4,5
		1	V	V	4	5	6	7	X	X	X	X	4	5	6	7	X	X	X	X	1,2,4,5
BL8	READ	0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	2
		0	0	1	1	2	3	0	5	6	7	4	1	0	3	2	5	4	7	6	2
		0	1	0	2	3	0	1	6	7	4	5	2	3	0	1	6	7	4	5	2
		0	1	1	3	0	1	2	7	4	5	6	3	2	1	0	7	6	5	4	2
		1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	2
		1	0	1	5	6	7	4	1	2	3	0	5	4	7	6	1	0	3	2	2
		1	1	0	6	7	4	5	2	3	0	1	6	7	4	5	2	3	0	1	2
		1	1	1	7	4	5	6	3	0	1	2	7	6	5	4	3	2	1	0	2
	WRITE	V	V	V	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	2,4

NOTE 1 In the case of setting burst length to BC4 (fixed) in MR0, the internal WRITE operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In the case of setting burst length to on-the-fly in MR0, the internal WRITE operation starts at the same point in time as a BL8 (even if BC4 was selected during column time using A12/$\overline{BC}$.). This means that if the on-the-fly MR0 setting is used, the starting point for tWR and tWTR will not be pulled in by two clocks as described in the BC4 (fixed) case.

NOTE 2 Bit number (B0…B7) is the value of column address CA [2:0] that causes this bit to be the first READ during a burst.

NOTE 3 T = Output driver for data and strobes are in High-Z.

NOTE 4 V = Valid logic level (0 or 1), but respective buffer input ignores level on input pins.

NOTE 5 X = "Don't Care."

BL8 Burst order with CRC Enabled

DDR4 SDRAM supports fixed write burst ordering [A2:A1: A0=0:0:0] when write CRC is enabled in BL8 (fixed)

DLL-off Mode and DLL on/off Switching procedure

DLL On/Off Switching Procedure

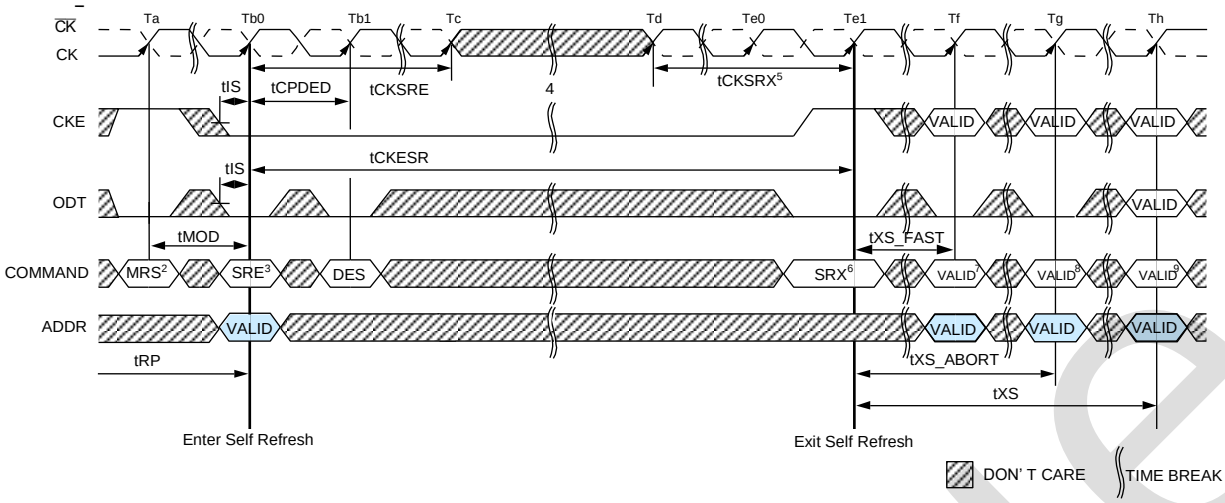
DDR4 DLL-off mode is entered by setting MR1 bit A0 to “0”; this will disable the DLL for subsequent operations until the A0 bit is set back to “1”.

DLL On to DLL Off Procedure

To switch from DLL “on” to DLL “off” requires the frequency to be changed during self refresh, as outlined in the following procedure:

1. Starting from the idle state (all banks pre-charged, all timings fulfilled, and DRAMs on-die termination resistors, RTT_NOM, must be in high impedance state before MRS to MR1 to disable the DLL.)
2. Set MR1 bit A0 to “0” to disable the DLL.
3. Wait tMOD.
4. Enter Self Refresh mode; wait until (tCKSRE) is satisfied.
5. Change frequency, following the guidelines in the “Input Clock Frequency Change” section.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when self refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If RTT_NOM was disabled in the mode registers when self refresh mode was entered, the ODT signal is "Don't Care."
8. Wait tXS_FASTor tXS_ABORT or tXS, and then set mode registers with appropriate values (especially an update of CL, CWL, and WR may be necessary; a ZQCL command can also be issued after tXS_FAST).
   - tXS: ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, RDAS8
   - tXS_FAST: ZQCL, ZQCS, MRS commands. For MRS commands, only CL and WR/RTP registers in MR0, the CWL register in MR2, and geardown mode in MR3 are allowed to be accessed provided the device is not in per-device addressability mode. Access to other device mode registers must satisfy tXS timing.
   - tXS_ABORT: If the MR4 bit A9 is enabled, then the DRAM aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command after a delay of tXS_ABORT. Upon exiting from self refresh, the DDR4 SDRAM requires a minimum of one extra REFRESH command before it is put back into self refresh mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.
9. Wait for tMOD, and then the DRAM is ready for the next command.

DLL Switch Sequence from DLL On to DLL Off



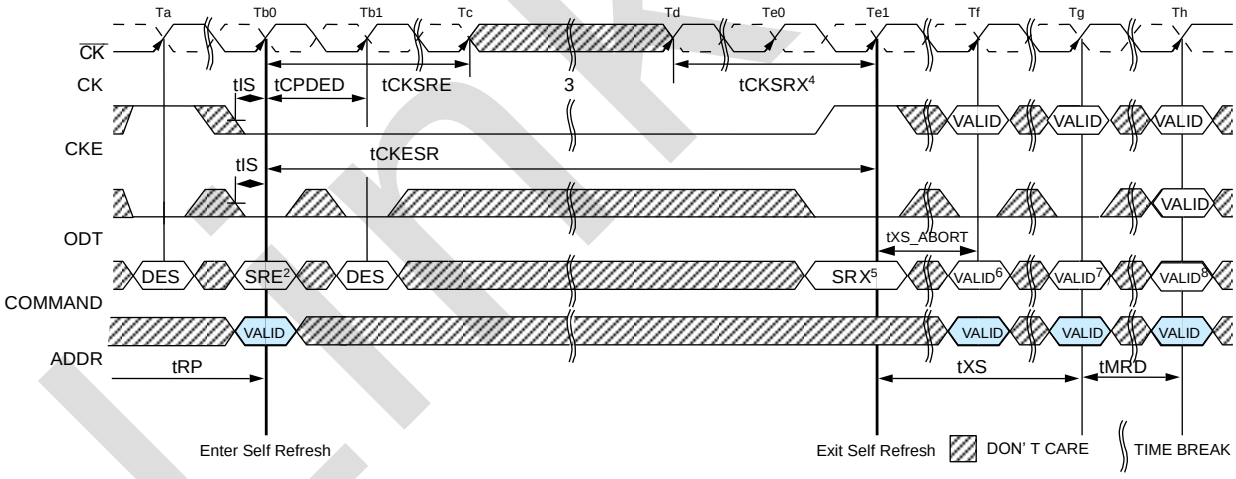
NOTE 1 Starting with idle state. RTT in stable.
NOTE 2 Disable DLL by setting MR1 bit A0 to "0".
NOTE 3 Enter SR.
NOTE 4 Change frequency.
NOTE 5 Clock must be stable in tCKSRX.
NOTE 6 Exit SR.
NOTE 7 Update mode registers allowed with DLL_off parameters setting.

DLL Off to DLL On Procedure

To switch from DLL off to DLL on (with required frequency change) during self refresh:

1. Starting from the idle state (all banks pre-charged, all timings fulfilled, and DRAM on-die termination resistors (RTT_NOM) must be in the high impedance state before self refresh mode is entered.)
2. Enter Self Refresh mode; wait until tCKSRE satisfied.
3. Change frequency, following the guidelines in the “Input Clock Frequency Change” section.
4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from the subsequent DLL RESET command is satisfied. In addition, if any ODT features were enabled in the mode registers when self refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from the subsequent DLL RESET command is satisfied. If RTT_NOM was disabled in the mode registers when self refresh mode was entered, the ODT signal is "Don't Care."
6. Wait tXS or tXS_ABORT, depending on bit A9 in MR4, then set MR1 bit A0 to “1” to enable the DLL.
7. Wait tMRD, then set MR0 bit A8 to “1” to start DLL Reset.
8. Wait tMRD, then set mode registers with appropriate values (especially an update of CL, CWL, and WR may be necessary. After tMOD is satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)
9. Wait for tMOD, then DRAM is ready for the next command. (Remember to wait tDLLK after DLL RESET before applying any command requiring a locked DLL.) In addition, wait for tZQoper in case a ZQCL command was issued.

DLL Switch Sequence from DLL Off to DLL On



NOTE 1 Starting with idle state.
NOTE 2 Enter SR.
NOTE 3 Change frequency.
NOTE 4 Clock must be stable tCKSRX.
NOTE 5 Exit SR.
NOTE 6,7 Set DLL on by setting MR1 A0 = “1”.
NOTE 8 Start DLL reset
NOTE 9 Update rest MR register values after tDLLK (not shown in the diagram)
NOTE 10 Ready for valid command after tDLLK (not shown in the diagram)

DLL-Off Mode

DLL-off mode is entered by setting MR1 bit A0 to “0”, this will disable the DLL for subsequent operations until the A0 bit is set back to “1”. The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to “Input Clock Frequency Change” for more details.

The DLL-off Mode operations listed below are an optional feature for DDR4 SDRAM. The maximum clock frequency for DLL-off mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

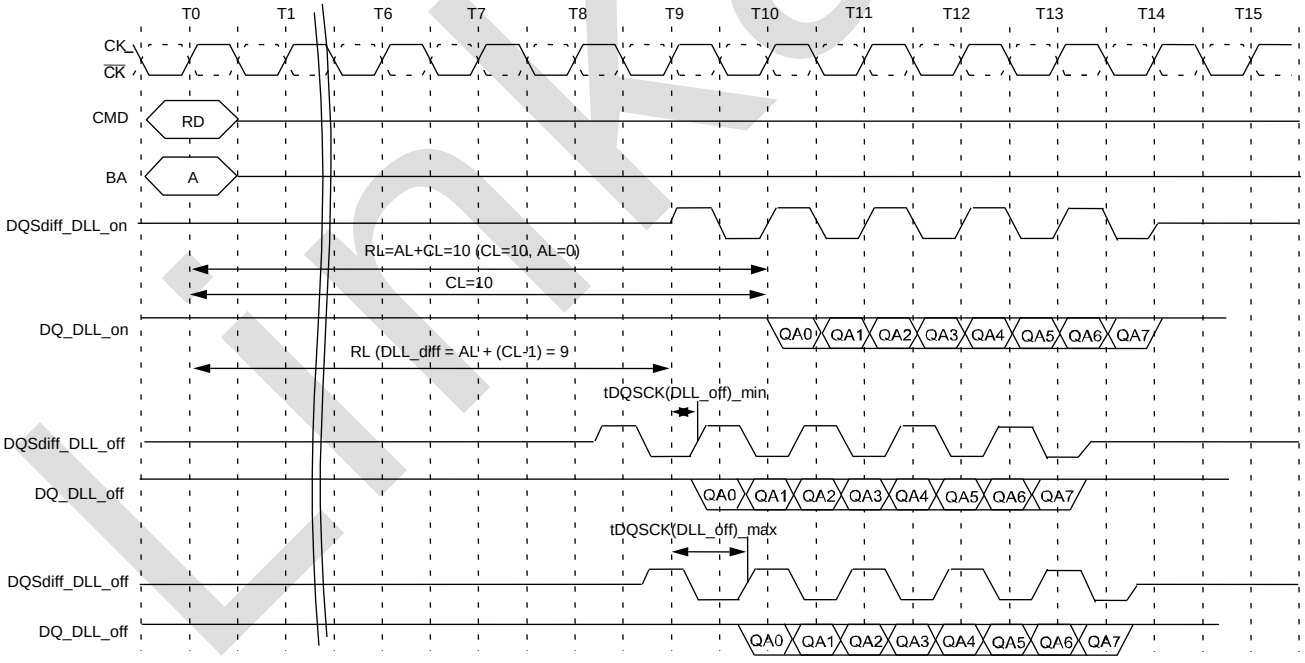
Due to latency counter and timing restrictions, only one CL value in MR0 and CWL in MR2 are supported. The DLL-off mode is only required to support setting both CL = 10 and CWL = 9.

When DLL-off Mode is enabled, use of CA Parity Mode is not allowed. DLL-off mode will affect the read data clock-to-data strobe relationship (tDQSCK), but not the data strobe-to-data relationship (tDQSQ, tQH). Special attention is needed to line up read data to the controller time domain.

Compared with DLL-on mode, where tDQSCK starts from the rising clock edge (AL + CL) cycles after the READ command, the DLL-off mode tDQSCK starts (AL + CL - 1) cycles after the READ command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK), and the difference between tDQSCK MIN and tDQSCK MAX is significantly larger than in DLL-on mode. The tDQSCK (DLL_off) values are vendor-specific.

READ operation at DLL-off mode

(CL=10, BL=8, PL=0)



Input Clock Frequency Change

Once the DDR4 SDRAM is initialized, the DDR4 SDRAM requires the clock to be stable during almost all states of normal operation. This means that after the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications. The input clock frequency can be changed from one stable clock rate to another stable clock rate under self refresh mode. Outside of self refresh mode, it is illegal to change the clock frequency.

Once the DDR4 SDRAM has been successfully placed in self refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don’t care. Once a “don’t care”, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting self refresh mode for the sole purpose of changing the clock frequency, the self refresh entry and exit specifications must still be met as outlined in “Self-Refresh Operation”.

For the new clock frequency, additional MRS commands to MR0, MR2, MR3, MR4, MR5, and MR6 may need to be issued to program appropriate CL, CWL, Gear-down mode, Read & Write Preamble, Command Address Latency (CAL Mode), Command Address Parity (CA Parity Mode), and tCCD_L/tDLLK value.

In particular, the Command Address Parity Latency (PL) must be disabled when the clock rate changes, i.e. while in Self Refresh Mode. For example, if changing the clock rate from DDR4-2133 to DDR4-2933 with CA Parity Mode enabled, MR5[2:0] must first change from PL = 4 to PL = disable prior to PL = 6. A correct procedure would be to (1) change PL = 4 to disable via MR5 [2:0], (2) enter Self Refresh Mode, (3) change clock rate from DDR4-2133 to DDR4-2933, (4) exit Self Refresh Mode, (5) Enable CA Parity Mode setting PL = 6 via MR5 [2:0].

If the MR settings that require additional clocks are updated after the clock rate has been increased, i.e. after exiting self refresh mode, the required MR settings must be updated prior to removing the DRAM from the IDLE state, unless the DRAM is RESET. If the DRAM leaves the idle state to enter self refresh mode or ZQ Calibration, the updating of the required MR settings may be deferred to after the next time the DRAM enters the IDLE state.

If MR6 is issued prior to Self Refresh Entry for new tDLLK value, then DLL will relock automatically at Self Refresh Exit. However, if MR6 is issued after Self Refresh Entry, then MR0 must be issued to reset the DLL.

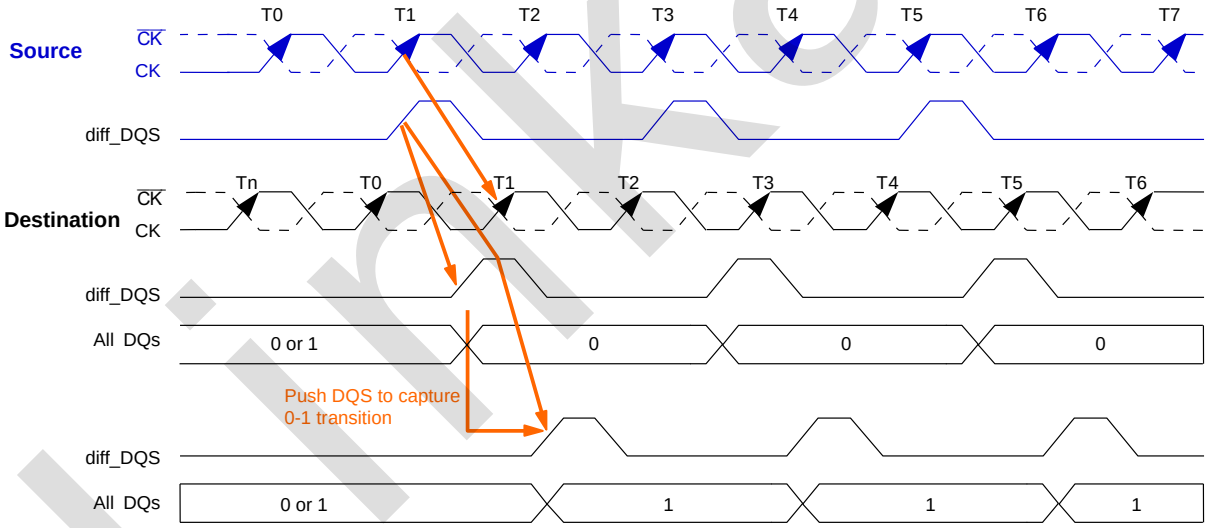
The DDR4 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on mode to DLL_off mode transition sequence (see DLL On/Off Switching Procedure).

Write Leveling

For better signal integrity, the DDR4 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR4 SDRAM supports a “write-leveling” feature to allow the controller to compensate for skew. This feature may not be required under some system conditions, provided the host can maintain the tDQSS, tDSS, and tDSH specifications.

The memory controller can use the write leveling feature and feedback from the DDR4 SDRAM to adjust the DQS - $\overline{DQS}$ to CK - $\overline{CK}$ relationship. The memory controller involved in the leveling must have an adjustable delay setting on DQS - $\overline{DQS}$ to align the rising edge of DQS - $\overline{DQS}$ with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK - $\overline{CK}$, sampled with the rising edge of DQS - $\overline{DQS}$, through the DQ bus. The controller repeatedly delays DQS - $\overline{DQS}$ until a transition from 0 to 1 is detected. The DQS - $\overline{DQS}$ delay established through this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS - $\overline{DQS}$ signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the “AC Timing Parameters” section in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown below.

Write-Leveling Concept



DQS - $\overline{DQS}$ driven by the controller during leveling mode must be terminated by the DRAM based on the ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits carry the leveling feedback to the controller across the DRAM configurations x4, x8, and x16. On a x16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS)-to-clock relationship; the lower data bits would indicate the lower diff_DQS(diff_LDQS)-to-clock relationship.

DRAM Setting for Write Leveling and DRAM Termination Function in that Mode

DRAM enters into write leveling mode if A7 in MR1 set “HIGH”, and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 is LOW (see the MR leveling table below). Note that in write leveling mode, only DQS/$\overline{\text{DQS}}$ terminations are activated and deactivated via the ODT pin, unlike normal operation (see DRAM termination table below).

MR Settings for Leveling Procedures

Function	MR1	Enable	Disable
Write Leveling enable	A7	1	0
Data output disable (Qoff)	A12	0	1

DRAM Termination Function in Leveling Mode

ODT Pin at DRAM	DQS/$\overline{\text{DQS}}$ Termination	DQ Termination
RTT_NOM with ODT HIGH	On	Off
RTT_PARK with ODT LOW	On	Off

NOTE 1 In write-leveling mode with its output buffer disabled (MR1[bit A7] = 1 with MR1[bit A12] =1) all RTT_NOM and RTT_PARK settings are allowed; in write-leveling mode with its output buffer enabled (MR1[bitA7] = 1 with MR1[bitA12] = 0) all RTT_NOM and RTT_PARK settings are allowed.

NOTE 2 Dynamic ODT function is not available in Write Leveling Mode. DRAM MR2 bits A [11:9] must be ‘000’ prior to entering Write Leveling Mode.

Procedure Description

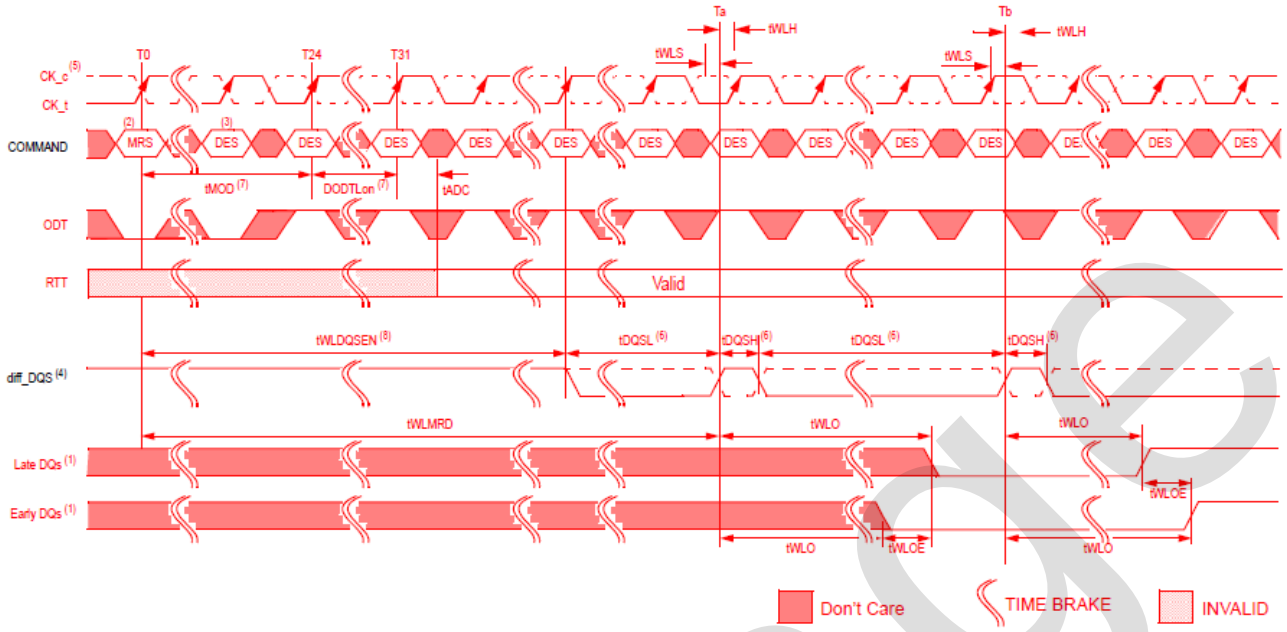
The memory controller initiates the leveling mode of all DRAM by setting bit A7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only the DESELECT commands are allowed, as well as an MRS command to change the Qoff bit (MR1[A12]) and an MRS command to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7] = 0) may also change MR1 bits of A12-A8, A2-A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal.

The controller may drive DQS LOW and $\overline{DQS}$ HIGH after a delay of tWLDQSEN, at which time the DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, the controller provides a single DQS, $\overline{DQS}$ edge which is used by the DRAM to sample CK - $\overline{CK}$ driven from the controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK - $\overline{CK}$ status with the rising edge of DQS - $\overline{DQS}$ and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS, $\overline{DQS}$) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS - $\overline{DQS}$ delay setting and launches the next DQS - $\overline{DQS}$ pulse after some time, which is controller dependent. After a 0-to-1 transition is detected, the controller locks the DQS - $\overline{DQS}$ delay setting, and write leveling is achieved for the device. The following figure shows the timing diagram and parameters for the overall write leveling procedure.

Parameter	Symbol	DDR4 1600/1866/2133/2400/2666/2933/3200		Units	NOTE
		Min	Max		
Write Leveling Output Error	tWLOE	0	2	ns	

Timing details of Write leveling sequence (DQS-$\overline{DQS}$ is capturing CK - $\overline{CK}$ low at Ta and CK - $\overline{CK}$ high at Tb)



NOTE 1 DDR4 SDRAM drives leveling feedback on all DQs

NOTE 2 MRS : Load MR1 to enter write leveling mode

NOTE 3 DES : Deselect

NOTE 4 diff_DQS is the differential data strobe (DQS-$\overline{DQS}$). Timing reference points are the zero crossings. DQS is shown with solid line, $\overline{DQS}$ is shown with dotted line

NOTE 5 CK/$\overline{CK}$: CK is shown with solid dark line, whereas $\overline{CK}$ is drawn with dotted line.

NOTE 6 DQS , $\overline{DQS}$ needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent

NOTE 7 tMOD(Min) = max(24nCK, 15ns), WL = 9 (CWL = 9, AL = 0, PL = 0), DODTLon = WL -2 = 7

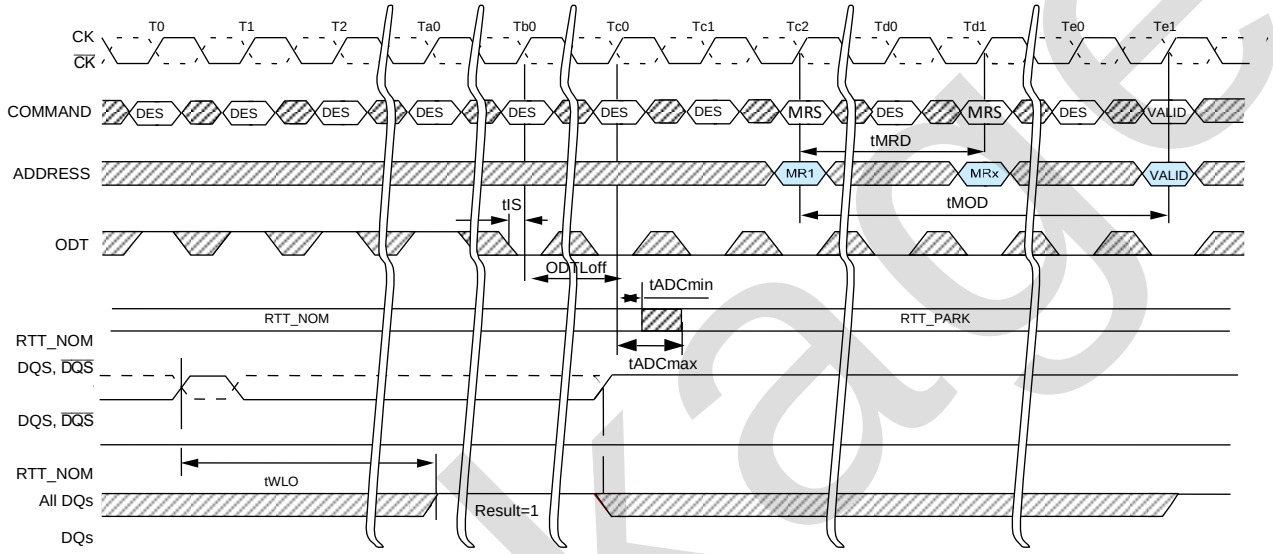
NOTE 8 tWLDQSEN must be satisfied following equation when using ODT.
tWLDQSEN > tMOD(Min) + ODTLon + tADC : at DLL = Enable
tWLDQSEN > tMOD(Min) + tAONAS : at DLL = Disable

Write-Leveling Mode Exit

Write leveling mode should be exited as follows:

1. After the last rising strobe edge (see T0), stop driving the strobe signals (see Tc0). Note that from this point now on, DQ pins are in undefined driving mode and will remain undefined, until tMOD after the respective MRS command (Te1).
2. Drive ODT pin LOW (tIS must be satisfied) and continue registering LOW (see Tb0).
3. After the RTT is switched off, disable write-leveling mode via the MRS command (see Tc2).
4. After tMOD is satisfied (Te1), any valid command can be registered. MR commands can be issued after tMRD (Td1).

Timing details of Write leveling exit



Temperature-Controlled Refresh Modes (TCR)

This mode is enabled and disabled by setting bit A3 in MR4. Two modes are supported that are selected by bit A2 setting in MR4.

Temperature range

Grade	Normal Temperature Mode	Extended Temperature Mode
Commercial grade (0°C ~ 95°C)	0<Tc ≤ 85°C	0<Tc ≤ 95°C
Industrial grade(-40°C ~ 95°C)	-40<Tc ≤ 85°C	-40°C <Tc ≤ 95°C
Quasi-industrial grade(-40°C ~ 95°C)	-40<Tc ≤ 85°C	-40°C <Tc ≤ 95°C

Normal temperature mode

Once this mode is enabled by setting bit A3=1 and A2=0 in MR4, Refresh commands should be issued to DDR4 SDRAM with the average periodic refresh interval (7.8us for 2Gb, 4Gb, 8Gb, and 16Gb device) which is tREFI of normal temperature range. In this mode, the system guarantees that the DRAM temperature does not exceed 85°C.
Below 45°C, DDR4 SDRAM may adjust internal average periodic refresh interval by skipping external refresh commands with proper gear ratio. Not more than three fourths of external refresh commands are skipped at any temperature in this mode.The internal average periodic refresh interval adjustment is automatically done inside the DRAM and user does not need to provide any additional control.

Extended temperature mode

Once this mode is enabled by setting bit A3=1 and A2=1 in MR4, Refresh commands should be issued to DDR4 SDRAM with the average periodic refresh interval (3.9us for 2Gb, 4Gb, 8Gb, and 16Gb device) which is tREFI of extended temperature range. In this mode, the system guarantees that the DRAM temperature does not exceed extended temperature range.
In the normal temperature range, DDR4 SDRAM adjusts its internal average periodic refresh interval to tREFI of the normal temperature range by skipping external refresh commands with proper gear ratio. Below 45°C, DDR4 SDRAM may further adjust internal average periodic refresh interval. Not more than seven eighths of external commands are skipped at any temperature in this mode. The internal average periodic refresh interval adjustment is automatically done inside the DRAM and user does not need to provide any additional control.

Normal tREFI Refresh (TCR Disabled)

Temperature	Normal Temperature		Extended Temperature	
	External Refresh Period	Internal Refresh Period	External Refresh Period	Internal Refresh Period
Tc <45°C	7.8µs	7.8µs	3.9µs(1)	3.9µs(1)
45≤Tc ≤85°C				
85<Tc ≤ 95°C	(Not Applicable)			

NOTE 1 If T_C is less than 85°C then the external refresh period can be 7.8µs instead of 3.9us.

Normal tREFI Refresh (TCR Enabled)

Temperature	Normal Temperature		Extended Temperature	
	External Refresh Period	Internal Refresh Period	External Refresh Period	Internal Refresh Period
Tc <45°C	7.8µs	≥ 7.8µs	3.9µs(1)	≥ 3.9µs
45≤Tc ≤85°C		7.8µs		≥ 3.9µs
85<Tc ≤ 95°C	(Not Applicable)			3.9µs

NOTE 1 DRAM might refresh internally at slow refresh rate and will violate refresh specifications.

Fine Granularity Refresh Mode (FGRM)

Mode Register and Command Truth Table

The REFRESH cycle time (tRFC) and the Average Refresh Interval (tREFI) of DDR4 SDRAM can be programmed by the MRS command. The appropriate setting in the mode register will set a single set of REFRESH cycle time and average refresh interval for the DDR4 SDRAM device (fixed mode), or allow the dynamic selection of one of two sets of REFRESH cycle time and average refresh interval for the DDR4 SDRAM device (on-the-fly mode, OTF). OTF mode must be enabled by MRS before any OTF REFRESH command can be issued.

MR3 definition for Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal mode (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 1x/2x
1	1	0	Enable on the fly 1x/4x
1	1	1	Reserved

There are two types of OTF modes (1x/2x and 1x/4x modes) that are selectable by programming the appropriate values into the mode register. When either of the two OTF modes is selected ('A8=1'), DDR4 SDRAM evaluates the BG0 bit when a REFRESH command is issued, and depending on the status of BG0, it dynamically switches its internal refresh configuration between 1x/2x or 1x/4x modes, then executes the corresponding REFRESH operation.

REFRESH Command Truth Table (OTF modes)

REFRESH	CS	$\overline{ACT}$	$\overline{RAS}$ /A16	$\overline{CAS}$ /A15	$\overline{WE}$ /A14	BG1	BG0	BA0-1	A10/ AP	A[9:0], A[12:11], A17	MR3 A[8:6]
Fixed rate	L	H	L	L	H	V	**V**	V	V	V	**0vv**
OTF – 1x	L	H	L	L	H	V	**L**	V	V	V	**1vv**
OTF – 2x	L	H	L	L	H	V	**H**	V	V	V	**101**
OTF – 4x											**110**