DDR4 SDRAM

P3AAG2BLF
P3AAG3BLF
P3AAG4BLF

F a

- $V_{DD} = V_{DDQ}$ = 1.2V ᴍ60mV
- V_{PP} = 2.5V, –125mV, +250mV
- On-die, internal, adjustable V_{REFDQ} generation
- 1.2V pseudo open-drain I/O
- T_C maximum up to 95JC
  – 64ms, 8192-cycle refresh up to 85JC
  – 32ms, 8192-cycle refresh at >85JC to 95JC
- 16 internal banks (x4, x8): 4 groups of 4 banks each
- 8 internal banks (x16): 2 groups of 4 banks each
- 8*n*-bit prefetch architecture
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination (ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Connectivity test
- JEDEC JESD-79-4 compliant
- sPPR and hPPR capability

O [1] Ma

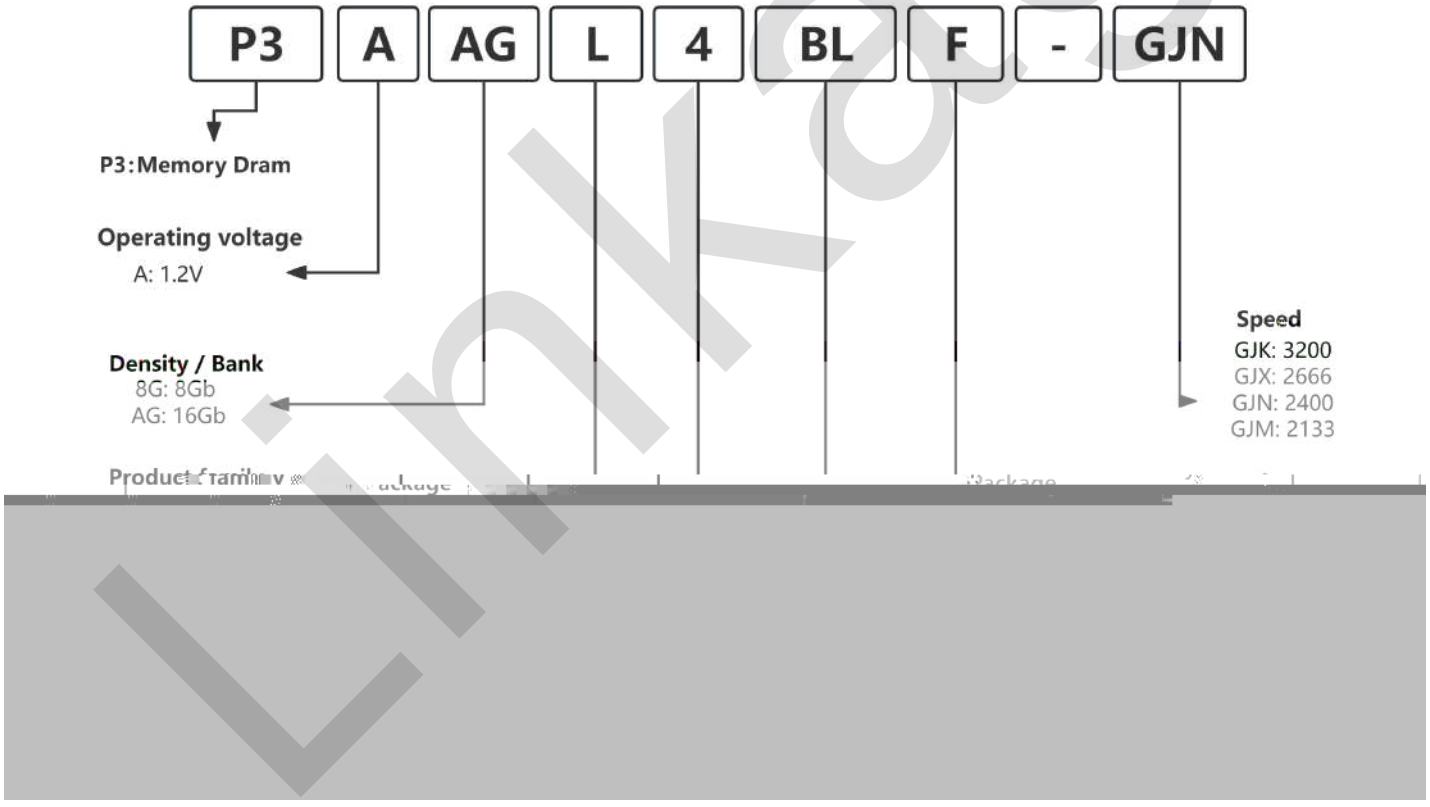
- Configuration
  – 4 Gig x 4 — 4G4
  – 2 Gig x 8 — 2G8
  – 1 Gig x 16 — 1G16
- Timing – cycle time
  – 0.625ns @ CL = 22 (DDR4-3200) — -GJK
  – 0.682ns @ CL = 21 (DDR4-2933) — -GJY
  – 0.750ns @ CL = 19 (DDR4-2666) — -GJX
  – 0.833ns @ CL = 17 (DDR4-2400) — -GJN
- Operating temperature
  – Commercial (0J S T_C S 95JC) — None
  – Industrial (–40J S T_C S 95JC) — IT

Add

Pa a	4096 M 4	2048 M 8	1024 M 16
Number of bank groups	4	4	2
Bank group address	BG[1:0]	BG[1:0]	BG0
Bank count per group	4	4	4
Bank address in bank group	BA[1:0]	BA[1:0]	BA[1:0]
Row addressing	256K (A[17:0])	128K (A[16:0])	128K (A[16:0])
Column addressing	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])
Page size[1]	512B	1KB	2KB

Notes: 1. Page size is per bank, calculated as follows:
Page size = $2^{COLBITS}$ ρ ORG/8, where COLBIT = the number of column address bits and ORG = the number of DQ bits.

F 1: O d Pa N b E a



G a N a d D c

D c

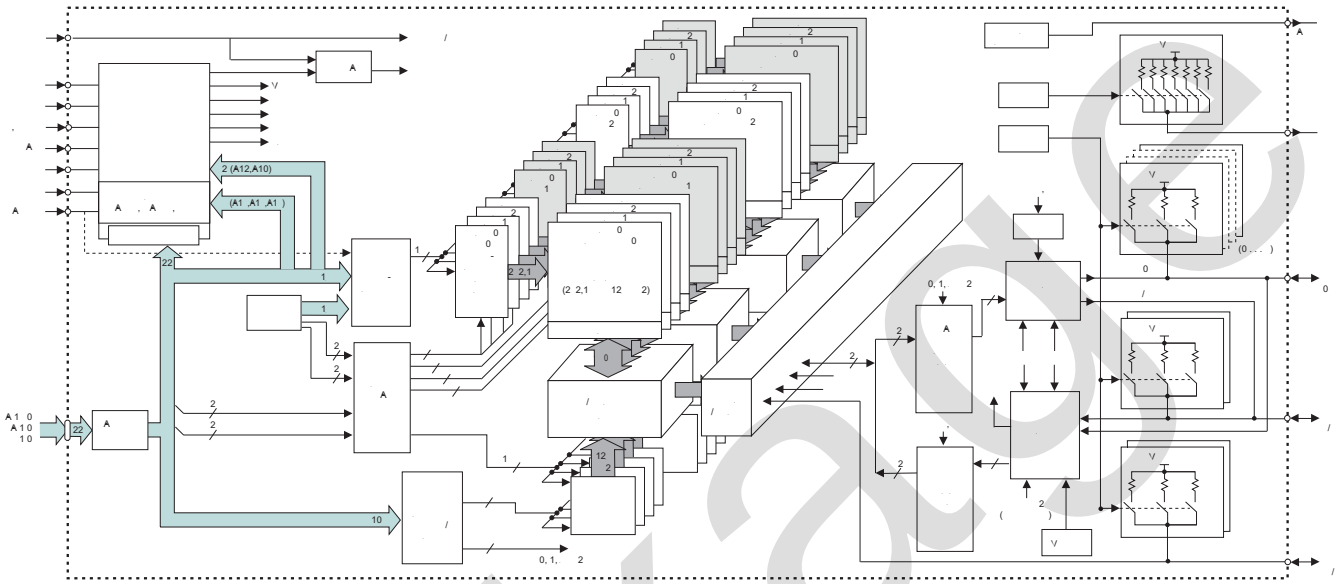
The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM for the x16 configuration and as a 16-bank DRAM for the x4 and x8 configurations. The DDR4 SDRAM uses an 8*n*-prefetch architecture to achieve high-speed operation. The 8*n*-prefetch

- Not all specifications listed are finalized industry standards; best conservative estimates have been provided when an industry standard has not been finalized.
- Although it is implied throughout the specification, the DRAM must be used after V_{DD} has reached

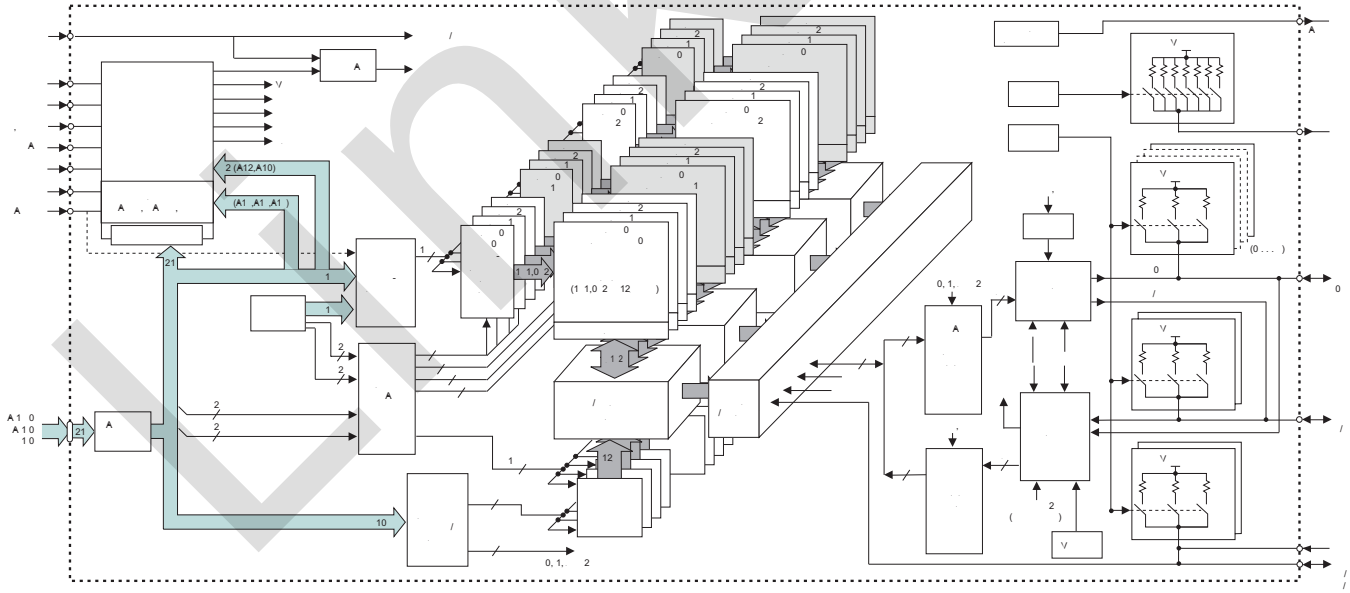
F c a B c D a a

DDR4 SDRAM is a high-speed, CMOS dynamic random access memory. It is internally configured as an 16-bank (4-banks per Bank Group) DRAM.

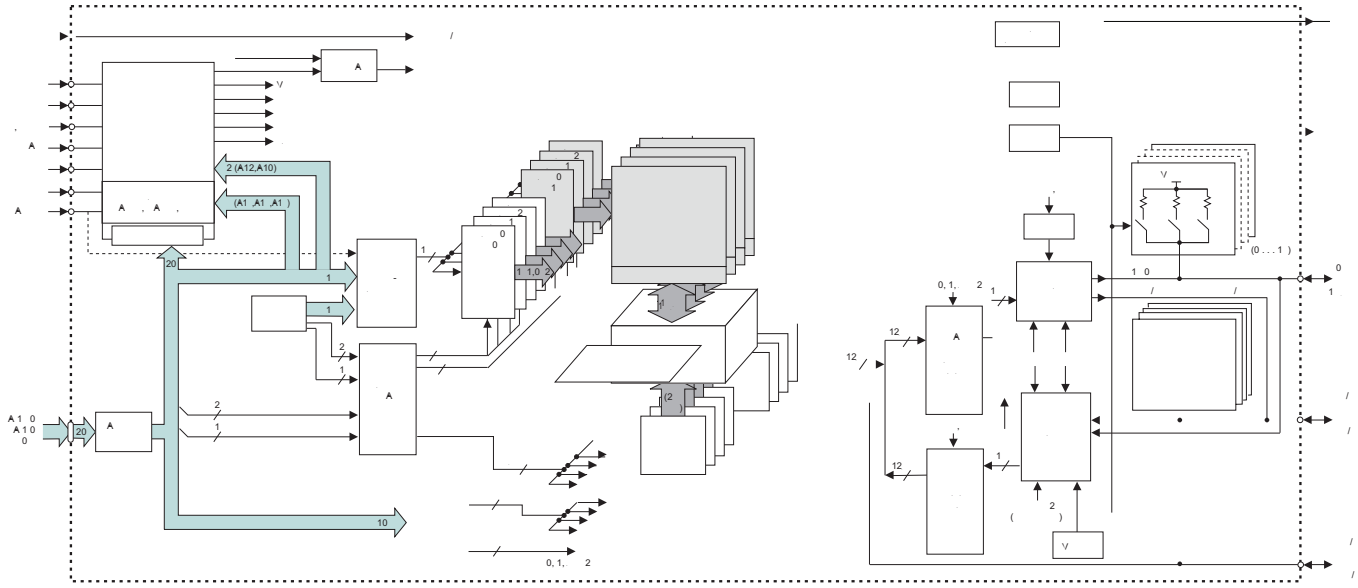
F 2: 4 G 4 F c a B c D a a



F 3: 2 G 8 F c a B c D a a

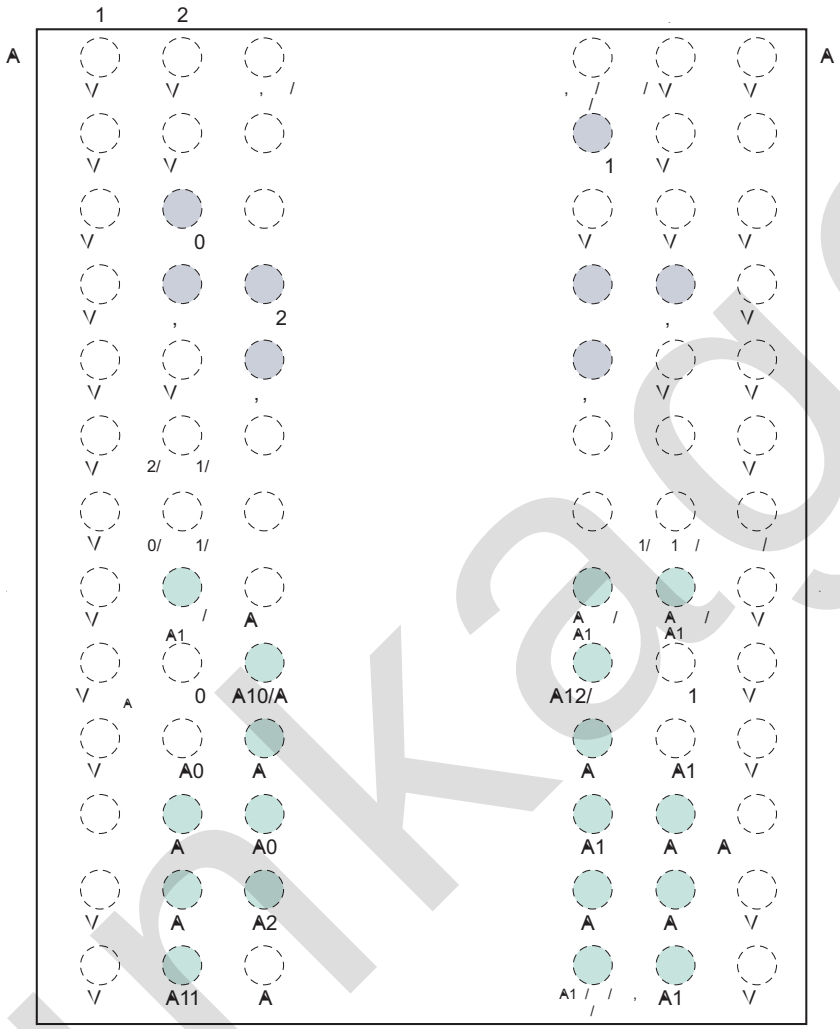


F 4: 1 G 16 F c a B c D a a



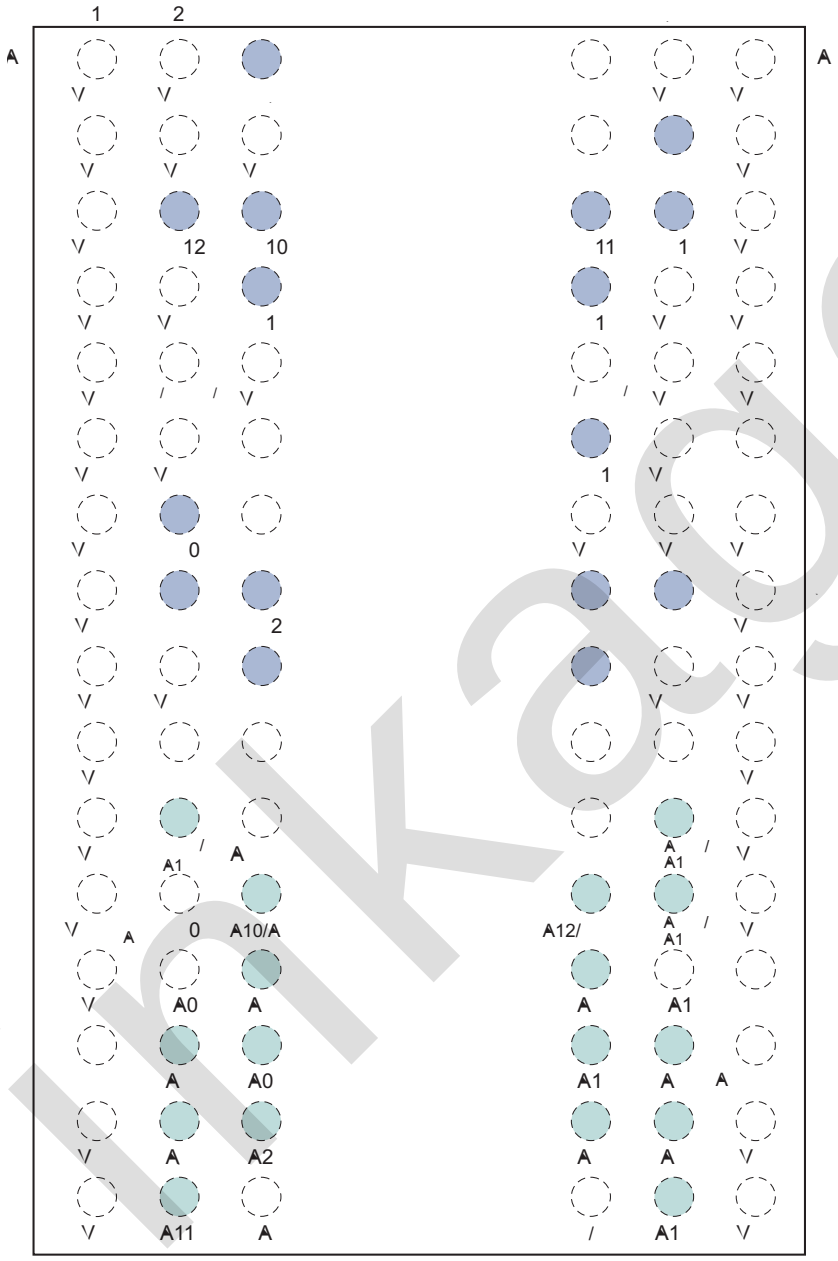
Ba A

F 5: 78-Ba 4, 8 Ba A



Notes: 1. See Ball Descriptions.
2. A comma "," separates the configuration; a slash "/" defines a mode register selectable function, command/address function, density, or package dependence.
3. Address bits (including bank groups) are density- and configuration-dependent (see Addressing).

F 6: 96-Ba 16 Ba A



Notes: 1. See Ball Descriptions.
2. A slash "/" defines a mode register selectable function, command/address function, density, or package dependence.
3. Address bits (including bank groups) are density- and configuration-dependent (see Addressing).

Ba D c

The pin description table below is a comprehensive list of all possible pins for DDR4 devices. All pins listed may not be supported on the device defined in this data sheet. See the Ball Assignments section to review all pins used on this device.

Ba D c

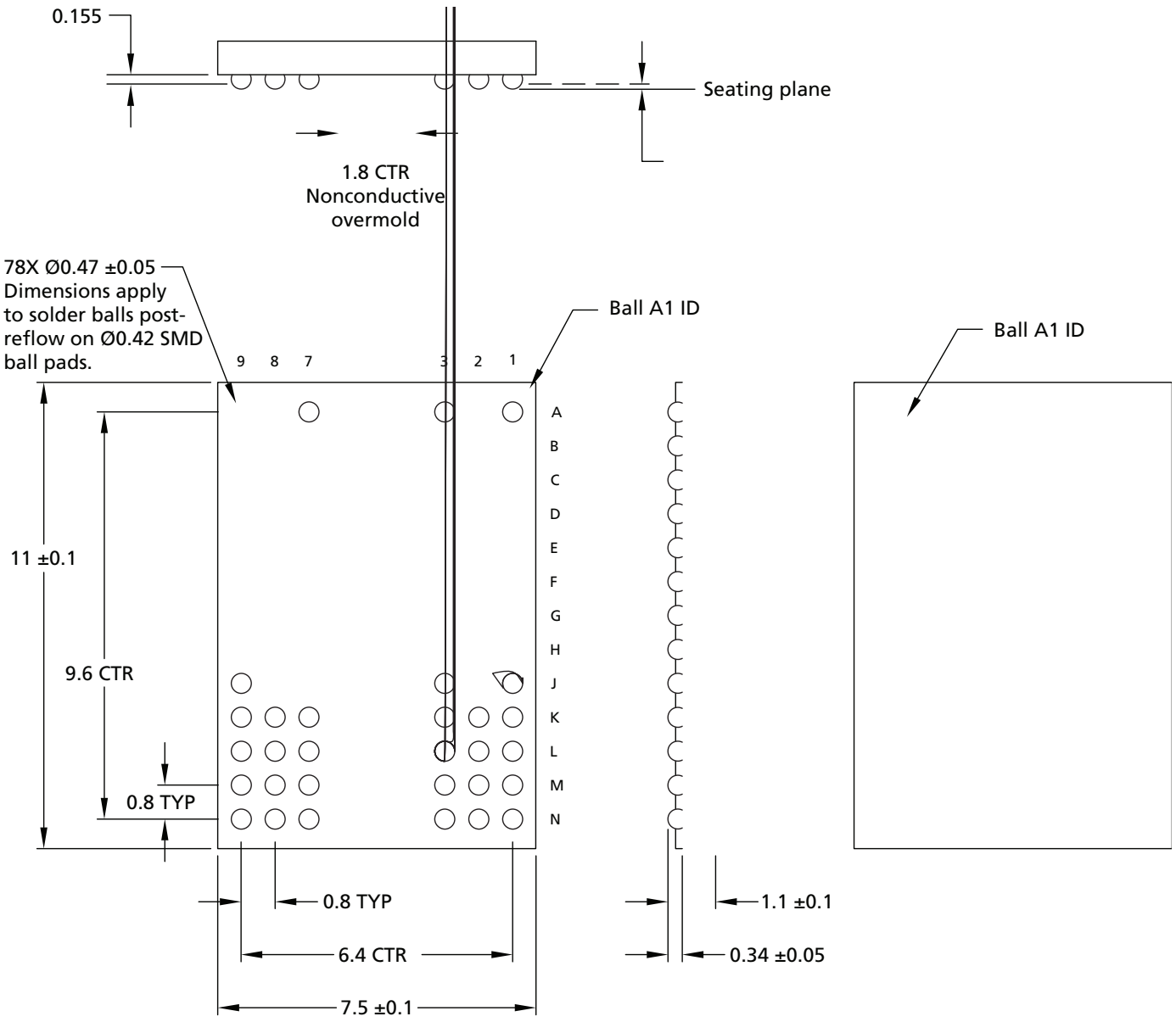
S b	T	D c
A[17:0]	Input	**Add :** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, RAS_n/A16 have additional functions, see individual entries in this table.) The address inputs also provide the op-code during the MODE REGISTER SET command. A16 is used on some 8Gb and 16Gb parts. A17 connection is part-number specific; Contact vendor for more information.
A10/AP	Input	**A c a :** A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation. (HIGH = auto precharge; LOW = no auto precharge.) A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**B c :** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed. (HIGH = no burst chop; LOW = burst chopped). See the Command Truth Table.
ACT_n	Input	**C a d :** ACT_n indicates an ACTIVATE command. When ACT_n (along with CS_n) is LOW, the input pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are treated as row address inputs for the ACTIVATE command. When ACT_n is HIGH (along with CS_n LOW), the input pins RAS_n/ A16, CAS_n/A15, and WE_n/A14 are treated as normal commands that use the RAS_n, CAS_n, and WE_n signals. See the Command Truth Table.
BA[1:0]	Input	**Ba add :** Define the bank (within a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command.
BG[1:0]	Input	**Ba add :** Define the bank group to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determines which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. BG1 is not used in the x16 configuration.
C0/CKE1, C1/CS1_n, C2/ODT1	Input	**S ac add :** These inputs are used only when devices are stacked; that is, they are used in 2H, 4H, and 8H stacks for x4 and x8 configurations (these pins are not used in the x16 configuration, and are NC on the x4/x8 SDP). DDR4 will support a traditional DDP package, which uses these three signals for control of the second die (CS1_n, CKE1, ODT1). DDR4 is not expected to support a traditional QDP package. For all other stack configurations, such as a 4H or 8H, it is assumed to be a single-load (master/slave) type of configuration where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT signal.
CK_t, CK_c	Input	**C c :** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.

CKE	Input	**C c ab :** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE

Ba D c (C d)

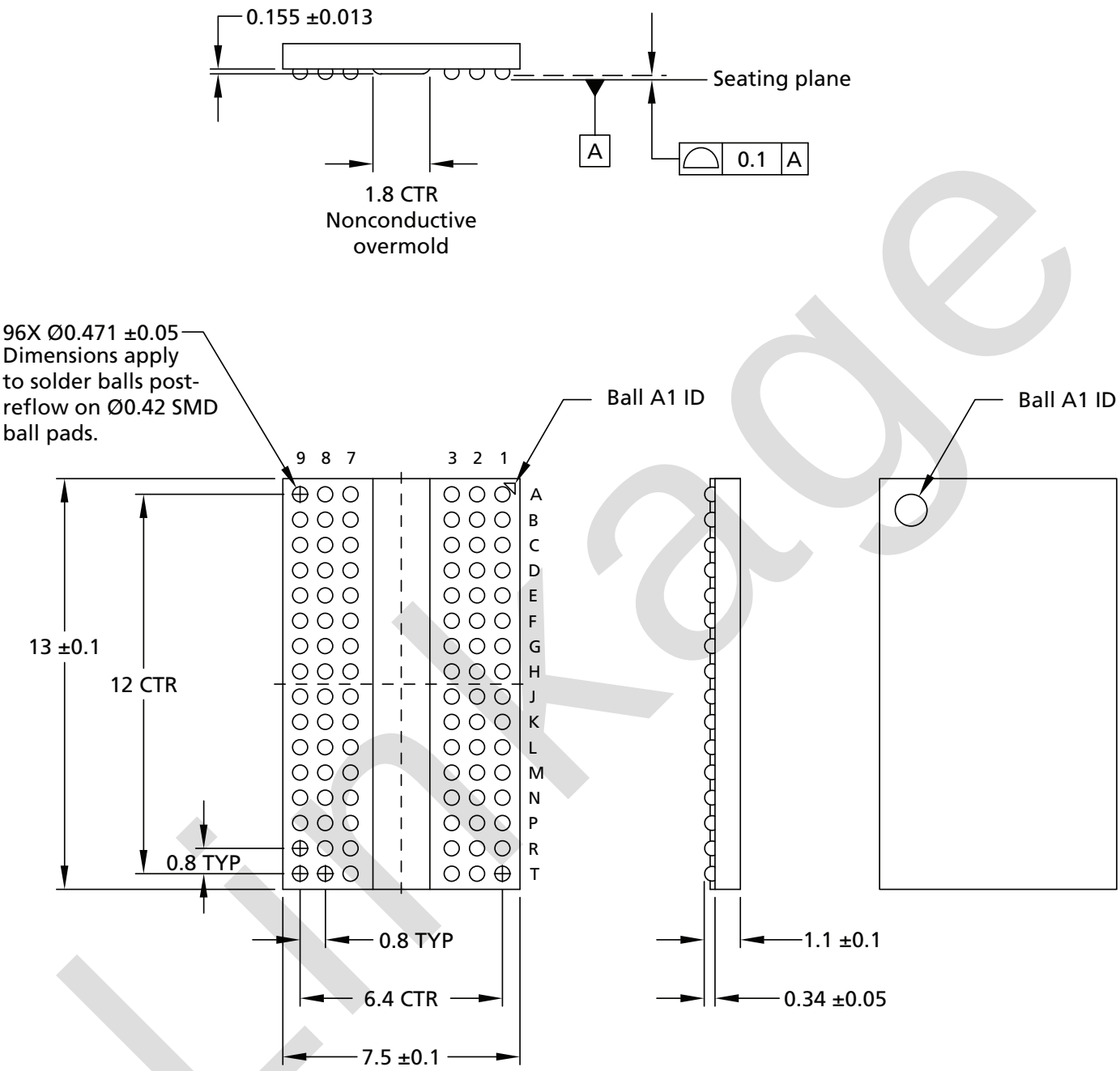
S b	T	D c
DQ	I/O	**Da a / :** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If write CRC is enabled via mode register, the write CRC code is added at the end of data burst. Any one or all of DQ0, DQ1, DQ2, and DQ3 may be used to monitor the internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH, training times change when enabled. During this mode, the R_{TT} value should be set to High-Z. This measurement is for verification purposes and is NOT an external voltage supply pin.
DBI_n, UDBI_n, LDBI_n	I/O	**DBI / :** Data bus inversion. DBI_n is an input/output signal used for data bus inversion in the x8 configuration. UDBI_n and LDBI_n are used in the x16 configuration; UDBI_n is associated with DQ[15:8], and LDBI_n is associated with DQ[7:0]. The DBI feature is not supported on the x4 configuration. DBI is not supported for 3DS devices and should be disabled in MR5. DBI can be configured for both READ (output) and WRITE (input) operations depending on the mode register settings. The DM, DBI, and TDQS functions are enabled by mode register settings. See the Data Bus Inversion section.
DQS_t, DQS_c, UDQS_t, UDQS_c, LDQS_t, LDQS_c	I/O	**Da a b :** Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITE data. For the x16, LDQS corresponds to the data on DQ[7:0]; UDQS corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	**A :** This signal allows the DRAM to indicate to the system's memory controller that a specific alert or event has occurred. Alerts will include the command/address parity error and the CRC data error when either of these functions is enabled in the mode register.
TDQS_t, TDQS_c	Output	**T a da a b :** TDQS_t and TDQS_c are used by x8 DRAMs only. When enabled via the mode register, the DRAM will enable the same R_{TT} termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin will provide the DATA MASK (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations.
V_{DD}	Supply	**P :** 1.2V ᴍ0.060V.
V_{DDQ}	Supply	**DQ :** 1.2V ᴍ0.060V.
V_{PP}	Supply	**DRAM ac a :** 2.5V –0.125V/+0.250V.
V_{REFCA}	Supply	Reference voltage for control, command, and address pins.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	DQ ground.
ZQ	Reference	**R c ba ZQ ca b a :** This ball is tied to an external 240ᴓ resistor (RZQ), which is tied to V_{SSQ}.
RFU	–	Reserved for future use.
NC	–	**N c c :** No internal electrical connection is present.
NF	–	**N c :** Internal connection is present but has no function.

78-Ball FBGA – x4, x8



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

96-Ball FBGA – x16



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

Sa Da a

This simplified state diagram provides an overview of the possible state transitions and the commands to control them. Situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

S dSa Da a

Sa Da a C a d D

C a d	D c
ACT	Active
MPR	Multipurpose register
MRS	Mode register set
PDE	Enter power-down
PDX	Exit power-down
PRE	Precharge
PREA	Precharge all
READ	RD, RDS4, RDS8
READ A	RDA, RDAS4, RDAS8
REF	Refresh, fine granularity refresh
RESET	Start reset procedure
SRE	Self refresh entry
SRX	Self refresh exit
TEN	Boundary scan mode enable
WRITE	WR, WRS4, WRS8 with/without CRC
WRITE A	WRA, WRAS4, WRAS8 with/without CRC
ZQCL	ZQ calibration long
ZQCS	ZQ calibration short

Notes: 1. See the Command Truth Table for more details.

F c a D c

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen banks (4 bank groups with 4 banks for each bank group) for x4/x8 devices, and as eight banks for each bank group (2 bank groups with 4 banks each) for x16 devices. The device uses double data rate (DDR) architecture to achieve high-speed operation. DDR4 architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for a device module effectively consists of a single 8*n*-bit-wide, four-clock-cycle-data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the device are burst-oriented. Accesses start at a selected location and continue for a burst length of eight or a chopped burst of four in a programmed sequence. Operation begins with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BG[1:0] select the bank group for x4/x8, and BG0 selects the bank group for x16; BA[1:0] select the bank, and A[17:0] select the row. See the Addressing section for more details). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst operation, determine if the auto PRECHARGE command is to be issued (via A10), and select BC4 or BL8 mode on-the-fly (OTF) (via A12) if enabled in the mode register.

Prior to normal operation, the device must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

NOTE: The use of the NOP command is allowed only when exiting maximum power saving mode or when entering gear-down mode.

RESET a d I a a P c d

To ensure proper device function, the power-up and reset initialization default values for the following mode register (MR) settings are defined as:

- Gear-down mode (MR3 A[3]): 0 = 1/2 rate
- Per-DRAM addressability (MR3 A[4]): 0 = disable
- Maximum power-saving mode (MR4 A[1]): 0 = disable
- CS to command/address latency (MR4 A[8:6]): 000 = disable
- CA parity latency mode (MR5 A[2:0]): 000 = disable
- Hard post package repair mode (MR4 A[13]): 0 = disable
- Soft post package repair mode (MR4 A[5]): 0 = disable

P -U a d I a a S A c

The following sequence is required for power-up and initialization:

1. Apply power (RESET_n and TEN should be maintained below 0.2 ρ V_{DD} while supplies ramp up; all other inputs may be undefined). When supplies have ramped to a valid stable level, RESET_n must be maintained below 0.2 ρ V_{DD} for a minimum of ^{t}PW_RESET_L and TEN must be maintained below 0.2 ρ V_{DD} for a minimum of 700As. CKE is pulled LOW anytime before RESET_n is de-asserted (minimum time of 10ns). The power voltage ramp time between 300mV to $V_{DD,min}$ must be no greater than 200ms, and during the ramp, V_{DD} must be greater than or equal to V_{DDQ} and (V_{DD} - V_{DDQ}) < 0.3V. V_{PP} must ramp at the same time or up to 10 minutes prior to V_{DD}, and V_{PP} must be equal to or higher than V_{DD} at all times. The total time for which V_{PP} is powered and V_{DD} is unpowered should not exceed 360 cumulative hours. After V_{DD} has ramped and reached a stable level, RESET_n must go high within 10 minutes. After RESET_n goes high, the initialization sequence

– Condition B:
  - Apply V_{PP} without any slope reversal before or at the same time as V_{DD}.
  - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}.
  - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} and V_{REFCA}.
  - The voltage levels on all pins other than V_{PP}, V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.

2. After RESET_n is de-asserted, wait for a minimum of 500As, but no longer than 3 seconds, before allowing CKE to be registered HIGH at clock edge Td. During this time, the device will start internal state initialization; this will be done independently of external clocks. A reasonable attempt was made in the design to power up with the following default MR settings: gear-down mode (MR3 A[3]): 0 = 1/2 rate; per-DRAM addressability (MR3 A[4]): 0 = disable; maximum power-down (MR4 A[1]): 0 = disable; CS to command/address latency (MR4 A[8:6]): 000 = disable; CA parity latency mode (MR5 A[2:0]): 000 = disable. However, it should be assumed that at power up the MR settings are undefined and should be programmed as shown below.
3. Clocks (CK_t, CK_c) need to be started and stabilized for at least 10ns or 5 ^{t}CK (whichever is larger) before CKE is registered HIGH at clock edge Td. Because CKE is a synchronous signal, the corresponding setup time to clock (^{t}IS) must be met. Also, a DESELECT command must be registered (with ^{t}IS setup time to clock) at clock edge Td. After the CKE is registered HIGH after RESET, CKE needs to be continuously registered HIGH until the initialization sequence is finished, including expiration of ^{t}DLLK and ^{t}ZQinit.
4. The device keeps its ODT in High-Z state as long as RESET_n is asserted. Further, the SDRAM keeps its ODT in High-Z state after RESET_n de-assertion until CKE is registered HIGH. The ODT input signal may be in an undefined state until ^{t}IS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held either LOW or HIGH. If $R_{TT(NOM)}$ is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power-up initialization sequence is finished, including the expiration of ^{t}DLLK and ^{t}ZQinit.
5. After CKE is registered HIGH, wait a minimum of RESET CKE EXIT time, ^{t}XPR, before issuing the first MRS command to load mode register (^{t}XPR = MAX (^{t}XS, 5 ρ ^{t}CK).
6. Issue MRS command to load MR3 with all application settings, wait ^{t}MRD.
7. Issue MRS command to load MR6 with all application settings, wait ^{t}MRD.
8. Issue MRS command to load MR5 with all application settings, wait ^{t}MRD.
9. Issue MRS command to load MR4 with all application settings, wait ^{t}MRD.
10. Issue MRS command to load MR2 with all application settings, wait ^{t}MRD.
11. Issue MRS command to load MR1 with all application settings, wait ^{t}MRD.
12. Issue MRS command to load MR0 with all application settings, wait ^{t}MOD.
13. Issue a ZQCL command to start ZQ calibration.
14. Wait for ^{t}DLLK and ^{t}ZQinit to complete.
15. The device will be ready for normal operation. Once the DRAM has been initialized, if the DRAM is in an idle state longer than 960ms, then either (a) REF commands must be issued within ^{t}REFI constraints (specification for posting allowed) or (b) CKE or CS_n must toggle once within every 960ms interval of idle time. For debug purposes, the 960ms delay limit maybe extended to 60 minutes provided the DRAM is operated in this debug mode for no more than 360 cumulative hours.
16. Optional MBIST-PPR mode can be entered by setting MR4:A0 to 1, followed by subsequent MR0 guard key sequences, then DRAM will drive ALERT_n to LOW. DRAM will drive ALERT_n to HIGH

to indicate that this operation is completed. MBIST-PPR mode can take place anytime after Tk. Note that no exit sequence or re-initialization is needed after MBIST completes; As soon as ALERT_N goes HIGH and ^{t}IS is satisfied, MR0 must be re-written to the pre guard key state, then and the DRAM is immediately ready to receive valid commands.

A stable valid V_{DD} level is a set DC level (0Hz to 250 KHz) and must be no less than $V_{DD,min}$ and no greater than $V_{DD,max}$. If the set DC level is altered anytime after initialization, the DLL reset and calibrations must be performed again after tl7.3t

Notes: 1. From time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
2. MRS commands must be issued to all mode registers that have defined settings.
3. In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).
4. TEN is not shown; however, it is assumed to be held LOW.
5. Optional MBIST-PPR may be entered any time after Tk.

RESET I a a S ab P S c

The following sequence is required for RESET at no power interruption initialization:

1. Assert RESET_n below 0.2 ρ V_{DD} any time when reset is needed (all other inputs may be undefined).

   RESET_n needs to be maintained for minimum ^{t}PW_RESET. CKE is pulled LOW before RESET_n being de-asserted (minimum time 10ns).
2. Follow Steps 2 through 10 in the Reset and Initialization Sequence at Power-On Ramping procedure.

When the reset sequence is complete, all counters except the refresh counters have been reset and the device is ready for normal operation.

F 7: RESET P c d a P S ab C d

Notes: 1. From time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
2. MRS commands must be issued to all mode registers that have defined settings.

3. In general, there is no specific sequence for setting the MRS locations (except for dependent or co-related features, such as ENABLE DLL in MR1 prior to RESET DLL in MR0, for example).
4. TEN is not shown; however, it is assumed to be held LOW.

U c d P -D S A c

In the event of an uncontrolled ramping down of V_{PP} supply, V_{PP} is allowed to be less than V_{DD} provided the following conditions are met:

- Condition A: V_{PP} and V_{DD}/V_{DDQ} are ramping down (as part of turning off) from normal operating levels.
- Condition B: The amount that V_{PP} may be less than V_{DD}/V_{DDQ} is less than or equal to 500mV.
- Condition C: The time V_{PP} may be less than V_{DD} is S10ms per occurrence with a total accumulated time in this state S100ms.
- Condition D: The time V_{PP} may be less than 2.0V and above V_{SS} while turning off is S15ms per occurrence with a total accumulated time in this state S150ms.

E c ca S c ca

Ab Ra

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability. Although "unlimited" row accesses to the same row is allowed within the refresh period; excessive row accesses to the same row over a long term can result in degraded operation.

Ab Ma Ra

S b	Pa a	M	Ma	U	N
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–0.4	1.5	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.4	1.5	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	–0.4	3.0	V	3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.5	V	
T_{STG}	Storage temperature	–55	150	JC	2

Notes: 1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than 0.6 ρ V_{DDQ}. When V_{DD} and V_{DDQ} are <500mV, V_{REF} can be S300mV.
2. Storage temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to the JESD51-2 standard.
3. V_{PP} must be equal to or greater than V_{DD}/V_{DDQ} at all times when powered.

DRAM C O a T a Ra

Operating temperature, T_{OPER}, is the case surface temperature on the center/top side of the DRAM. For measurement conditions, refer to the JEDEC document JESD51-2.

T a Ra

S b	Pa a	M	Ma	U	N
T_{OPER}	Normal operating temperature range	-40	85	JC	1
	Extended temperature range (optional)	>85	105	JC	2

Notes: 1. The normal temperature range specifies the temperatures at which all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0JC to 85JC under all operating conditions for the commercial offering; The industrial and automotive temperature offerings allow the case temperature to go below 0JC to -40JC.
2. Some applications require operation of the commercial, industrial, and automotive temperature DRAMs in the extended temperature range (between 85JC and 105JC case temperature). Full specifications are supported in this range, but the following additional conditions apply:
   - Refer to tREFI and tRFC parameters table for tREFI requirements when operating above 85JC
   - If SELF REFRESH operation is required in the extended temperature range, it is mandatory to use either the manual self refresh mode with extended temperature range capability (MR2[6] = 0 and MR2 [7] = 1) or enable the optional auto self refresh mode (MR2 [6] = 1 and MR2 [7] = 1).

L a a

L a a

C d	S b	M	Ma	U	N
Input leakage (excluding ZQ and TEN)	I_{IN}	–2	2	AA	1
ZQ leakage	I_{ZQ}	–50	10	AA	1
TEN leakage	I_{TEN}	–6	10	AA	1, 2
V_{REFCA} leakage	I_{VREFCA}	–2	2	AA	3
Output leakage: $V_{OUT} = V_{DDQ}$	I_{OZpd}	–	10	AA	4

Notes: 1. Input under test $0V < V_{IN} < 1.1V$.
2. Additional leakage due to weak pull-down.
3. $V_{REFCA} = V_{DD}/2$, V_{DD} at valid level after initialization.
4. DQs are disabled.
5. ODT is disabled with the ODT input HIGH.

V_{REFCA} S

V_{REFCA} is to be supplied to the DRAM and equal to $V_{DD}/2$. The V_{REFCA} is a reference supply input and therefore does not draw biasing current.

The DC-tolerance limits and AC-noise limits for the reference voltages V_{REFCA} are illustrated in the figure below. The figure shows a valid reference voltage $V_{REF(t)}$ as a function of time (V_{REF} stands for V_{REFCA}). $V_{REF(DC)}$ is the linear average of $V_{REF(t)}$ over a very long period of time (1 second). This average has to meet the MIN/MAX requirements. Furthermore, $V_{REF(t)}$ may temporarily deviate from $V_{REF(DC)}$ by no more than M1% V_{DD} for the AC-noise limit.

V_{REFDQ} V a Ra

The voltage levels for setup and hold time measurements are dependent on V_{REF}. V_{REF} is understood as $V_{REF(DC)}$, as defined in the above figure. This clarifies that DC-variations of V_{REF} affect the absolute

voltage a signal has to reach to achieve a valid HIGH or LOW level, and therefore, the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF(DC)}$ deviations from the optimum position within the data-eye of the input signals. This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (±1% of V_{DD}

V_{REFDQ} Ra

MR6[6] selects range 1 (60% to 92.5% of V_{DDQ}) or range 2 (45% to 77.5% of V_{DDQ}), and MR6[5:0] sets the V_{REFDQ} level, as listed in the following table. The values in MR6[6:0] will update the V_{DDQ} range and level independent of MR6[7] setting. It is recommended MR6[7] be enabled when changing the settings in MR6[6:0], and it is highly recommended MR6[7] be enabled when changing the settings in MR6[6:0] multiple times during a calibration routine.

V_{REFDQ} Ra a d L

MR6[5:0]	MR6[6] 0 = Ra 1	MR6[6] 1 = Ra 2	MR6[5:0]	MR6[6] 0 = Ra 1	MR6[6] 1 = Ra 2
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 11 1111 are reserved		

S d B Tab

DDR4 DRAM timing is primarily covered by two types of tables: the Speed Bin tables in this section and the tables found in the Electrical Characteristics and AC Timing Parameters section. The timing parameter tables define the applicable timing specifications based on the speed rating. The Speed Bin tables on the following pages list the ^{t}AA, ^{t}RCD, ^{t}RP, ^{t}RAS, and ^{t}RC limits of a given speed mark and are

E c ca C a ac c a d AC T Pa a

E c ca C a ac c a d AC T Pa a : DDR4-1600 DDR4-2400

Pa a		S b	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		U	N
			M	Ma	M	Ma	M	Ma	M	Ma		
C c T												
Clock period average (DLL off mode)		^{t}CK (AVG, DLL_OFF)	8	20	8	20	8	20	8	20	ns	
Clock period average		^{t}CK (AVG, DLL_ON)	1.25	1.9	1.071	1.9	0.937	1.9	0.833	1.9	ns	3 , 13
High pulse width average		^{t}CH (AVG)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	^{t}CK (AVG)	
Low pulse width average		^{t}CL (AVG)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	^{t}CK (AVG)	
Clock period jitter	Total	^{t}JITper_tot	–63	63	–54	54	–47	47	–42	42	ps	17 , 18
	Deterministic	^{t}JITper_dj	–31	31	–27	27	–23	23	–21	21	ps	17
	DLL locking	^{t}JITper,lck	–50	50	–43	43	–38	38	-33	33	ps	
Clock absolute period		^{t}CK (ABS)	MIN = ^{t}CK (AVG) MIN + ^{t}JITper_tot MIN; MAX = ^{t}CK (AVG) MAX + ^{t}JITper_tot MAX								ps	
Clock absolute high pulse width (includes duty cycle jitter)		^{t}CH (ABS)	0.45	–	0.45	–	0.45	–	0.45	–	^{t}CK (AVG)	
Clock absolute low pulse width (includes duty cycle jitter)		^{t}CL (ABS)	0.45	–	0.45	–	0.45	–	0.45	–	^{t}CK (AVG)	
Cycle-to-cycle jitter	Total	^{t}JITcc _tot	–	125	–	107	–	94	–	83	ps	
	DLL locking	^{t}JITcc,lck	–	100	–	86	–	75	–	67	ps	

Cumulative error across 2 cycles t

E c ca C a ac c a d AC T Pa a : DDR4-1600 DDR4-2400 (C d)

Pa a	S b	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		U	N
		M	Ma	M	Ma	M	Ma	M	Ma		
Data Valid Window per device: ^{t}QH - ^{t}DQSQ each device's output per UI	$^{t}DVW_{d}$	0.63		0.63		0.64		0.64		UI	
Data Valid Window per device, per pin: ^{t}QH - ^{t}DQSQ each device's output per UI	$^{t}DVW_{p}$	0.66	–	0.66	–	0.69	–	0.72	–	UI	
DQ Low-Z time from CK_t, CK_c	^{t}LZDQ	–450	225	–390	195	–360	180	–330	175	ps	
DQ High-Z time from CK_t, CK_c	^{t}HZDQ	–	225	–	195	–	180	–	175	ps	
DQ S b I T											
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 1^{t}CK preamble	$^{t}DQSS_{1ck}$	–0.27	0.27	–0.27	0.27	–0.27	0.27	–0.27	0.27	CK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge for 2^{t}CK preamble	$^{t}DQSS_{2ck}$	NA		NA		NA		–0.50	0.50	CK	
DQS_t, DQS_c differential input low pulse width	^{t}DQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	CK	
DQS_t, DQS_c differential input high pulse width	^{t}DQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	CK	
DQS_t, DQS_c differential input high pulse width for 2^{t}CK preamble	^{t}DQSH2PRE	NA		NA		NA		1.46	-	CK	
DQS_t, DQS_c falling edge setup to CK_t, CK_c rising edge for 1^{t}CK preamble	$^{t}DSS_{1ck}$	0.18	–	0.18	–	0.18	–	0.18	–	CK	
DQS_t, DQS_c falling edge setup to CK_t, CK_c rising edge for 2^{t}CK preamble	$^{t}DSS_{2ck}$	NA		NA		NA		0	-	CK	
DQS_t, DQS_c falling edge hold from CK_t, CK_c rising edge for 1^{t}CK preamble	$^{t}DSH_{1ck}$	0.18	–	0.18	–	0.18	–	0.18	–	CK	
DQS_t, DQS_c falling edge hold from CK_t, CK_c rising edge for 2^{t}CK preamble	$^{t}DSH_{2ck}$	NA		NA		NA		0	-	CK	
DQS_t, DQS_c differential WRITE preamble for 1^{t}CK preamble	$^{t}WPRE_{1ck}$	0.9	–	0.9	–	0.9	–	0.9	–	CK	
DQS_t, DQS_c differential WRITE preamble for 2^{t}CK preamble	$^{t}WPRE_{2ck}$	NA		NA		NA		1.8	–	CK	
DQS_t, DQS_c differential WRITE postamble	^{t}WPST	0.33	–	0.33	–	0.33	–	0.33	–	CK	
DQS S b O T (DLL ab d)											