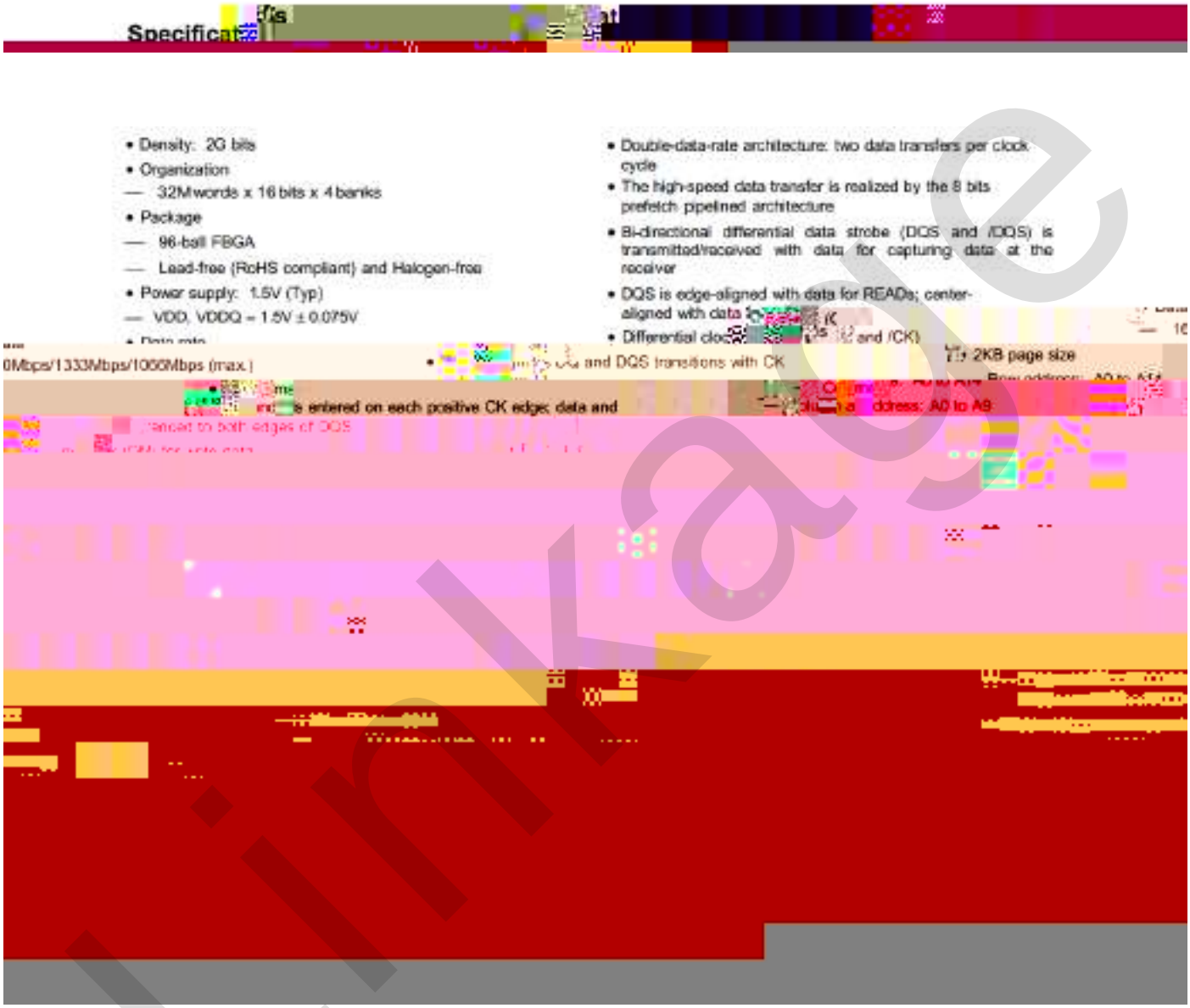
2G bits DDR3 SDRAM

P2P2GF4ALF-GGN（128M words X 16bits）



Ordering Information

Part number	Die revision	Organization (words × bits)	Internal banks	JEDEC speed b (CL-tRCD-t

Part Number

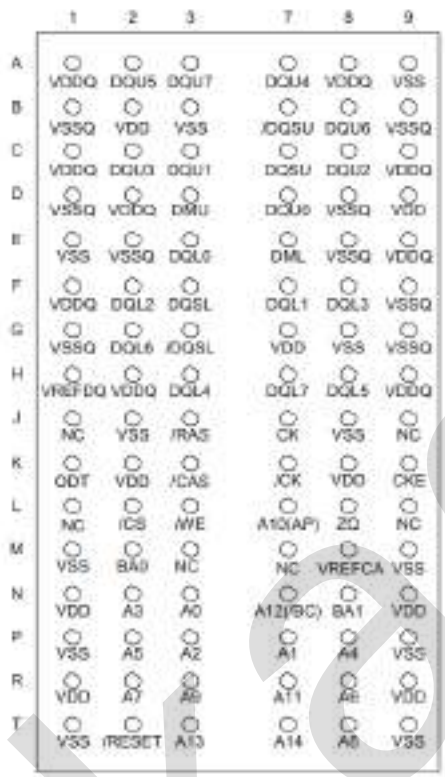
P 2 P 2 G F 4 A – L G G N

Pin Configurations

Pin Configurations (x 16 configuration)

/xxx indicates active low signal.

96-ball FBGA



(Top view)

CONTENTS

1. Electrical Conditions

- All voltages are referenced to VSS (GND)
- Execute power-up and Initialization sequence before proper device operation is achieved.

1.1 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Power supply voltage	VDD	–0.4 to +1.975	V	1, 3
Power supply voltage for output	VDDQ	–0.4 to +1.975	V	1, 3
Input voltage	VIN	–0.4 to +1.975	V	1
Output voltage	VOUT	–0.4 to +1.975	V	1
Reference voltage	VREFCA	–0.4 to 0.6 × VDD	V	3
Reference voltage for DQ	VREFDQ	–0.4 to 0.6 × VDDQ	V	

1.2 Operating Temperature Condition

Table 2: Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating case temperature	TC	0 to +95	°C	1, 2, 3

Notes: 1. Operating temperature is the case surface temperature on the center/top side of the
2. The Normal Temperature Range specifies the temperatures
operations will be supported. During
temperature must be
temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
requirement may not apply for some devices.)
(a) If Self-refresh operation is re
Self-Refresh mode with Exte
ired in the Extended Temperature Range, then it is mandatory to either use the Manual
ded Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto

1.5 IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined.
The figure Measurement Setup and Test Load for IDD and IDDQ Measurements shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.

Note: IDDQ values cannot be directly used to calculate I/O power of the DDR3 SDRAM. They can be used to support correlation of simulated I/O power to actual I/O power as outlined in correlation from simulated channel I/O power to actual channel I/O power supported by IDDQ measurement.

For IDD and IDDQ measurements, the following definitions apply:

- L and 0: VIN ≤ VIL(AC)max
- H and 1: VIN ≥ VIH(AC)min

- Basic IDD and IDDQ measurement conditions are described in Basic IDD and IDDQ Measurement Conditions
- The IDD and IDDQ measurement-loop patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Detailed IDD and IDDQ measurement-loop patterns are described in IDD0 Measurement-Loop Pattern table through IDD7 Measurement-Loop Pattern table.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting:
  - RON = RZQ/7 (34Ω in MR1);
  - Qoff = 0B (Output Buffer enabled in MR1);
  - RTT_Nom = RZQ/6 (40Ω in MR1);
  - RTT_WR = RZQ/2 (120Ω in
  - TDQS Feature disabled in M
- Define D = {/CS, /RAS, /CAS, /
- Define /D = {/CS, /RAS, /CA

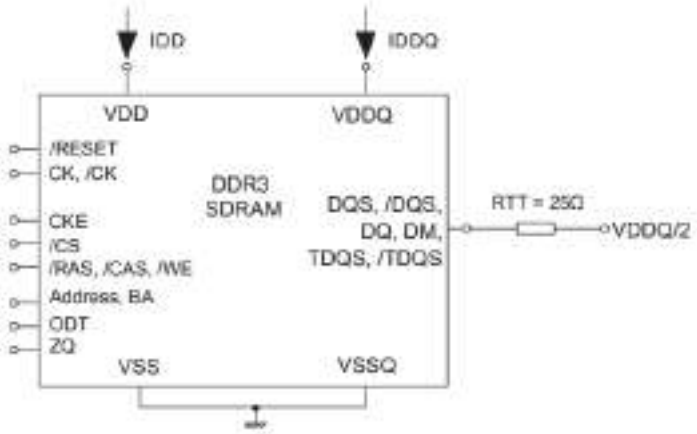


Figure 1: Measurement Setup and Test Load for IDD and IDDQ Measurements

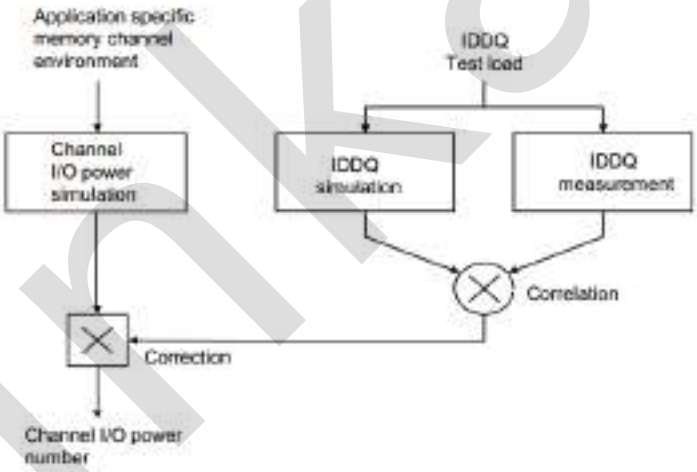


Figure 2: Correlation from Simulated Channel I/O Power to Actual Channel I/O Power Supported by IDDQ Measurement

1.5.1 Timings Used for IDD and IDDQ Measurement-Loop Patterns

Table 5: Timings Used for IDD and IDDQ Measurement-Loop Patterns

	DDR3-1066	DDR3-1333	DDR3-1600	
Parameter	**7-7-7**	**9-9-9**	**11-11-11**	**Unit**
CL	7	9	11	nCK
tCK(min)	1.875	1.5	1.25	ns
nRCD(min)	7	9	11	nCK
nRC(min)	27	33	39	nCK
nRAS(min)	20	24	28	nCK
nRP(min)	7	9	11	nCK
nFAW	27	30	32	nCK
nRRD	6	5	6	nCK
nRFC	139	174	208	nCK

1.5.2 Basic IDD and IDDQ Measurement Conditions

Table 6: Basic IDD and IDDQ Measurement Conditions

Parameter	Symbol	Description
Precharge power-down current fast exit	IDD2P1	CKE: L; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: MID-LEVEL; DM:stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; precharge power down mode: fast exit*3
Precharge quiet standby current	IDD2Q	CKE: H; External clock: On; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0;bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Active standby current	IDD3N	CKE: H; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 8; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 8
Active power-down current	IDD3P	CKE: L; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address inputs: stable at 0; data I/O: MID-LEVEL; DM:stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Operating burst read current	IDD4R	CKE: H; External clock: on; tCK, CL: see Table 4; BL: 8*1, *6; AL: 0; /CS: H between RD; Command, address, bank address Inputs: partially toggling according to Table 10; data I/O: seamless read data burst with different data between one burst and the next one according to Table 10; DM: stable at 0; bank activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 10); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 10
Operating burst read IDDQ current	IDDQ4R	Same definition like for IDD4R, however measuring IDDQ current instead of IDD current

RESET low current	IDD8	/RESET: low; External clock: off; CK and /CK: low; CKE: FLOATING; /CS, command, address, bank address, Data IO: FLOATING; ODT signal: FLOATING RESET low current reading is valid once power is stable and /RESET has been low for at least 1ms.

Notes: 1. Burst Length: BL8 fixed by MRS: MR0 bits [1,0] = [0,0].
2. MR: Mode Register
Output buffer enable: set MR1 bits [12, 5, 1] = [0, 1, 1]. RTT_Nom enable: set MR1 bits [10, 9, 6] = [0, 1, 1]. RTT_WR enable: set MR2 bits [10, 9] = [1,0].
3 Pre
4 A

Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.
2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.
3. BA: BA0 to BA1.

Table 10: IDD2N and IDD3N Measurement-Loop Pattern

CK, /CK	CKE	Sub-Loop	Cycle number	Command	/CS	/RAS	/CAS	/WE	ODT	BA[2:0][3]	A[15:13]	A12 /BC	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	DM[1]	DQS, /DQS[1]	DQ[1,2]
0	D	0	0	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		2	2	/D	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING.
2. DQ signals are FLOATING.
3. BA: BA0 to BA1.

Table 12: IDD4R and IDDQ4R Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA[*1]	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data[*2]
		0	0	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	0	0	0	0	0	—
			2,3	/D, /D	1	1	1	1	0	0	0	0	0	0	0	—
			4	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	0	0	0	F	0	—
			6,7	/D, /D	1	1	1	1	0	0	0	0	0	F	0	—
Toggling	Static H	1	8 to 15	Repeat Sub-Loop 0, but BA= 1												
		2	16 to 23	Repeat Sub-Loop 0, but BA= 2												
		3	24 to 31	Repeat Sub-Loop 0, but BA= 3												

Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.
2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.
3. BA: BA0 to BA1.

Table 13: IDD4W Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA[*3]	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data[*2]
		0	0	WR	0	1	0	0	1	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	0	0	0	0	0	—
			2,3	/D, /D	1	1	1	1	1	0	0	0	0	0	0	—
			4	WR	0	1	0	0	1	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	0	0	0	F	0	—
			6,7	/D, /D	1	1	1	1	1	0	0	0	0	F	0	—
Toggling	Static H	1	8 to 15	Repeat Sub-Loop 0, but BA= 1												
		2	16 to 23	Repeat Sub-Loop 0, but BA= 2												
		3	24 to 31	Repeat Sub-Loop 0, but BA= 3												

Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to write commands, otherwise FLOATING.
2. Burst se[illegible]
3. BA: BA[illegible] BA

Notes: 1. DM must be driven low all the time. DQS, /DQS are FLOATING.
2. DQ signals are FLOATING.
3. BA: BA0 to BA1.

Table 15: IDD7 Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA[3]	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data[2]
Toggling	Static H	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	—
			1	RDA	0	1	0	1	0	0	0	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	0	0	0	0	0	—
			...	Repeat above D Command until nRRD – 1												
		1	nRRD	ACT	0	0	1	1	0	1	0	0	0	F	0	—
			nRRD + 1	RDA	0	1	0	1	0	1	0	1	0	F	0	00110011
			nRRD + 2	D	1	0	0	0	0	1	0	0	0	F	0	—
			...	Repeat above D Command until 2 × nRRD – 1												
		2	2 × nRRD	Repeat Sub-Loop 0, but BA= 2												
		3	3 × nRRD	Repeat Sub-Loop 1, but BA= 3												
		4	4 × nRRD	D	1	0	0	0	0	3	0	0	0	F	0	—
				Assert and repeat above D Command until nFAW – 1, if necessary												
		5	nFAW	Repeat Sub-Loop 0, but BA= 4												
		6	nFAW + nRRD	Repeat Sub-Loop 1, but BA= 5												
		7	nFAW + 2 × nRRD	Repeat Sub-Loop 0, but BA= 6												
		8	nFAW + 3 × nRRD	Repeat Sub-Loop 1, but BA= 7												
		9	nFAW	D	1	0	0	0	0	7	0	0	0	F	0	—
			+ 4 × nRRD	Assert and repeat above D Command until 2 × nFAW – 1, if necessary												
		10	2 × nFAW + 0	ACT	0	0	1	1	0	0	0	0	0	F	0	—
			2 × nFAW + 1	RDA	0	1	0	1	0	0	0	1	0	F	0	00110011
		11	2 × nFAW + 2	D	1	0	0	0	0	0	0	0	0	F	0	—
				Repeat above D Command until 2 × nFAW + nRRD – 1												
			2 × nFAW + nRRD	ACT	0	0	1	1	0	1	0	0	0	0	0	—
			2 × nFAW + nRRD + 1	RDA	0	1	0	1	0	1	0	1	0	0	0	00000000
			2 × nFAW + nRRD + 2	D	1	0	0	0	0	1	0	0	0	0	0	—
				Repeat above D Command until 2 × nFAW + 2 × nRRD – 1												
		12	2 × nFAW +2 × nRRD	Repeat Sub-Loop 10, but BA= 2												
		13	2 × nFAW + 3 × nRRD	Repeat Sub-Loop 11, but BA= 3												
		14	2 × nFAW	D	1	0	0	0	0	3	0	0	0	0	0	—
			+ 4 × nRRD	Assert and repeat above D Command until 3 × nFAW – 1, if necessary												

Notes: 1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.
2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.
3. BA: BA0 to BA1.

2. Electrical Specifications

2.1 DC Characteristics

Table 16: DC Characteristics 1 (VDD, VDDQ = 1.5V± 0.075V)

Parameter	Symbol	Data rate (Mbps)	X16 max	Unit	Notes
Operating current (ACT-PRE)	IDD0	1066	55	mA	
		1333	60		
		1600	65		
Operating current (ACT-RD-PRE)	IDD1	1066	70	mA	
		1333	75		
		1600	80		
Precharge power-down standby current	IDD2P1	1066	30	mA	Fast PD Exit
		1333	35		
		1600	40		
	IDD2P0	1066	20	mA	Slow PD Exit
		1333	20		
		1600	20		
Precharge standby current	IDD2N	1066	45	mA	
		1333	45		
		1600	45		
Precharge standby ODT current	IDD2NT	1066	45	mA	
		1333	45		
		1600	45		
Precharge quiet standby current	IDD2Q	1066	40	mA	
		1333	45		
		1600	50		
Active power-down current (Always fast exit)	IDD3P	1066	37	mA	
		1333	39		
		1600	41		
Active standby current	IDD3N	1066	50	mA	
		1333	55		
		1600	60		
Operating current (Burst read operating)	IDD4R	1066	125	mA	
		1333	135		
		1600	145		
Operating current (Burst write operating)	IDD4W	1066	135	mA	
		1333	145		
		1600	155		
Burst refresh current	IDD5B	1066	250	mA	
		1333	250		
		1600	250		
All bank interleave read current	IDD7	1066	210	mA	
		1333	220		
		1600	230		
RESET low current	IDD8		17	mA	

Table 17: Self-Refresh Current (VDD, VDDQ = 1.5V± 0.075V)

Parameter	Symbol	max	Unit	Notes
Self-refresh current normal temperature range	IDD6	12	mA	
Self-refresh current extended temperature range	IDD6ET	25	mA	

2.2 Pin Capacitance

Table 18: Pin Capacitance [DDR3-1066 to 1600] (TC = 25°C, VDD, VDDQ = 1.5V± 0.075V)

		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units	Notes
Input/output capacitance	CIO	1.4	2.7	1.4	2.5	1.4	2.3	pF	1, 2
Input capacitance, CK and /CK	CCK	0.8	1.6	0.8	1.4	0.8	1.4	pF	2
Input capacitance delta, CK and /CK	CDCK	0	0.15	0	0.15	0	0.15	pF	2, 3
Input/output capacitance delta, DQS and /DQS	CDDQS	0	0.2	0	0.15	0	0.15	pF	2, 4
Input capacitance, (control, address, command, input-only pins)	CI	0.75	1.35	0.75	1.3	0.75	1.3	pF	2, 5
Input capacitance delta, (All control input-only pins)	CDI_CTRL	–0.5	0.3	–0.4	0.2	–0.4	0.2	pF	2, 6, 7
Input capacitance delta, (All addres/command input-only pins)	CDI_ADD_CMD	–0.5	0.5	–0.4	0.4	–0.4	0.4	pF	2, 8, 9
Input/output capacitance delta, DQ,DM, DQS, /DQS, TDQS, /TDQS	CDIO	–0.5	0.3	–0.5	0.3	–0.5	0.3	pF	2, 10
Input/output capacitance of ZQ pin	CZQ	—	3	—	3	—	3	pF	2, 11

Notes: 1. Although the DM, TDQS and /TDQS pins have different functions, the loading matches DQ and DQS.
2. VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, /RESET and ODT as necessary). VDD = VDDQ = 1.5V, VBIAS=VDD/2 and on-die termination off.
3. Absolute value of CCK-C/CK.
4. Absolute value of CIO(DQS)-CIO(/DQS).
5. CI applies to ODT, /CS, CKE, A0-A14, BA0-BA1, /RAS, /CAS and /WE.
6. CDI_CTRL applies to ODT, /CS and CKE.
7. CDI_CTRL = CI(CTRL) – 0.5 × (CI(CK)+CI(/CK)).
8. CDI_ADD_CMD applies to A0-A14, BA0-BA1, /RAS, /CAS and /WE.
9. CDI_ADD_CMD = CI(ADD_CMD) – 0.5 × (CI(CK)+CI(/CK)).
10. CDIO=CIO(DQ,DM) – 0.5 × (CIO(DQS)+CIO(/DQS)).
11. Maximum external load capacitance on ZQ pin: 5pF.

2.3 Standard Speed Bins

Table 19: DDR3-1066 Speed Bins

Speed Bin		DDR3-1066			
CL-tRCD-tRP		7-7-7			
Symbol	CAS write latency	min	max	Unit	Notes
tAA		13.125	20	ns	9
tRCD		13.125	—	ns	9
tRP		13.125			

Table 20: DDR3-1333 Speed Bins

Speed Bin		DDR3-1333			
CL-tRCD-tRP		9-9-9			
Symbol	tCAS write latency	min	max		
	CWL= 7	1.5	< 1.875	ns	1, 2, 3
Supported CL settings					
Supported CWL s					

Table 21: DDR3-1600 Speed Bins

Speed Bin		DDR3-1600			
CL-tRCD-tRP		11-11-11			
Symbol	/CAS write latency	min	max	Unit	Notes
tAA		13.75 (13.125)	20	ns	9
tRCD		13.75 (13.125)	—	ns	9
tRP		13.75 (13.125)	—	ns	9
tRC		48.75 (48.125)	—	ns	9
tRAS		35	9 × tREFI	ns	8
tCK(avg) @CL=5	CWL = 5	3.0	3.3	ns	1, 2, 3, 4, 7
	CWL = 6, 7, 8	Reserved	Reserved	ns	4
tCK(avg) @CL=6	CWL = 5	2.5	3.3	ns	1, 2, 3, 7
	CWL = 6	Reserved	Reserved	ns	4
	CWL = 7, 8	Reserved	Reserved	ns	4
tCK(avg) @CL=7	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	ns	1, 2, 3, 4, 7
	CWL = 7	Reserved	Reserved	ns	4
	CWL = 8	Reserved	Reserved	ns	4
tCK(avg) @CL=8	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	ns	1, 2, 3, 7
	CWL = 7	Reserved	Reserved	ns	4
	CWL = 8	Reserved	Reserved	ns	4
tCK(avg) @CL=9	CWL = 5, 6	Reserved	Reserved	ns	4
	CWL = 7	1.5	< 1.875	ns	1, 2, 3, 4, 7
	CWL = 8	Reserved	Reserved	ns	4
tCK(avg) @CL=10	CWL = 5, 6	Reserved	Reserved	ns	4
	CWL = 7	1.5	< 1.875	ns	1, 2, 3, 7
	CWL = 8	Reserved	Reserved	ns	4
tCK(avg) @CL=11	CWL = 5, 6, 7	Reserved	Reserved	ns	4
	CWL = 8	1.25	< 1.5	ns	1, 2, 3
Supported CL settings		5, 6, 7, 8, 9, 10, 11		nCK	
Supported CWL settings		5, 6, 7, 8		nCK	

Notes: 1. The CL setting and CWL setting result in tCK(avg)min and tCK(avg)max requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.

2. tCK(avg)min limits: Since /CAS latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (3.0, 2.5, 1.875, 1.5, or 1.25ns) when calculating CL(nCK) = tAA(ns) / tCK(avg)(ns), rounding up to the next 'Supported CL'.

3. tCK(avg)max limits: Calculate tCK(avg) = tAA(max)/CL selected and round the resulting tCK(avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875ns or 1.25ns). This result is tCK(avg)max corresponding to CL selected.

ved' settings are not allowed. User must program a different value.

DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1066

Speed Bins which are not subject to production tests but verified by design/characterization.

h is not subject to production tests but verified by design/characterization.

on tests but verified by design/characterization.

ure (TC).

g to CL = 7 and CL = 9, tAA/tR

Speed Bins which is not subject to produ

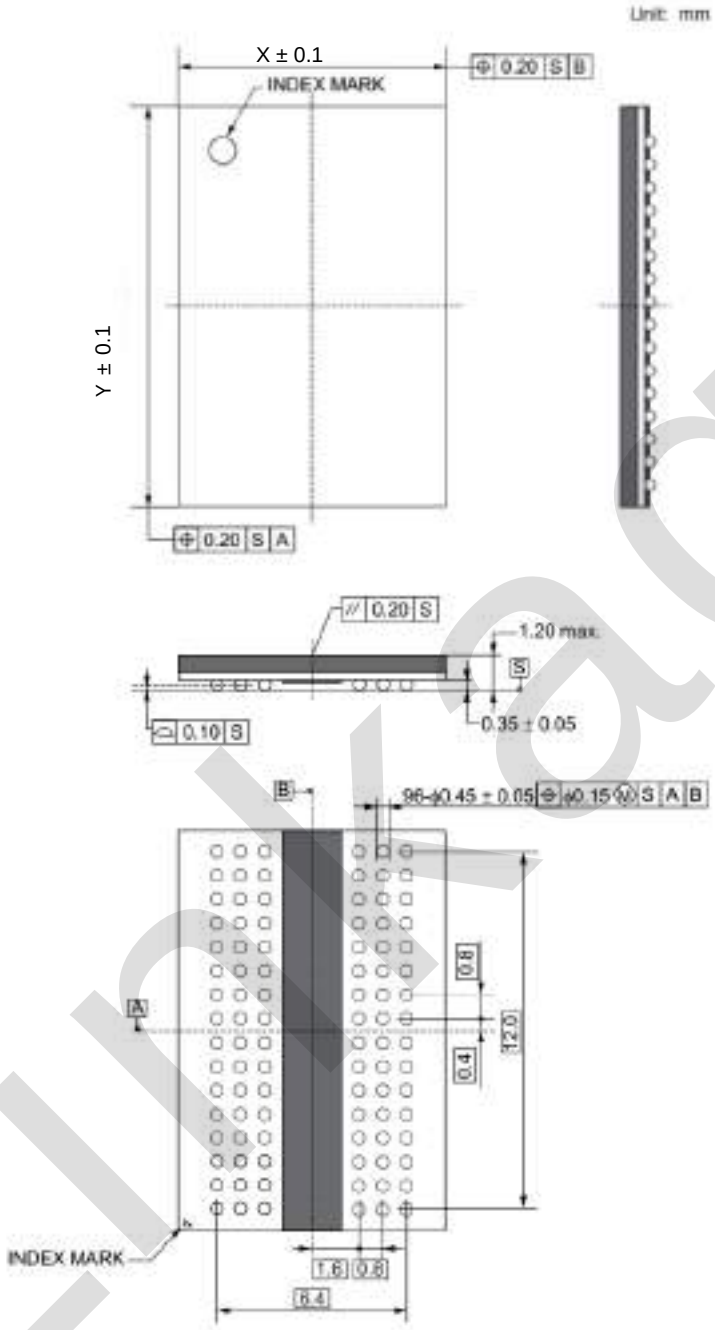
8. tREFI depends on operating case temper

9. For devices supporting optional down bin

programmed to match.

3. Package Drawing
3.1 96-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)



If X=7.5，so Y=13 or 13.3；
If X=8，so Y=13 or 14；
If X=9，so Y=13 or 13.5；

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifi